| Devi Ahilya University, Indore, India Institute of Engineering & Technology |        |                    |         | I Year M.E. (Computer Engineering<br>Sp. in Software Engineering )<br>(Full Time) |   |   |       |
|---|--------|--------------------|---------|---|---|---|-------|
| Subject Code & Name   | Instru | ctions How<br>Week | urs per | Credits   |   |   |       |
| SER1G3  | L      | Т                  | P       | L   | T | P | Total |
| ADVANCE COMPUTER<br>ARCHITECTURE  | 3      | 1                  | 0       | 3   | 1 | 0 | 4     |
| Duration of Theory Paper: 3 Hours   |        |                    |         |   |   |   |       |

### **Learning Objectives:**

- 1. To familiarize with current trends in high performance computing.
- 2. To introduce quantitative analysis of computer architectures

Pre requisites: Computer organization

## **Unit 1: Introduction to Computer Architeture & Quantitative Analysis**

Generations of Computers, Definition of Computer Architecture, General trends in technology, power and cost. Measuring, Reporting, and Summarizing performance. Quantitative principles of computer design.

#### **Unit 2: Pipelining & Instruction level Parallelism**

Need of pipelining, Pipeline Hazards, Implementation issues, Overcoming Pipeline hazards, pipeline extension to support multicycle operations. Concepts and challenges in ILP, Compiler techniques for ILP, Dynamic Scheduling, Hardware based Speculation, Combining dynamic scheduling, multiple issue and speculation.

#### **Unit 3: Memory Hierarchy Design**

Introduction, Optimizations for improving Cache performance, Memory technology and optimizations, Virtual Memory protection and performance issues, Virtual machines protection.

### Unit 4: Data level Parallelism and Thread level Parallelism

Introduction, Vector architecture, Graphics Processing Units, Detecting and enhancing loop-level parallelism, Centralized shared memory architecture, Shared Memory multiprocessors performance, distributed shared memory and directory-based coherence, models of memory consistency.

#### **Unit 5: Interconnection Networks**

Introduction, Connecting two or more devices, network topology, network routing, arbitration, and switching, Examples of interconnection networks, internetworking issues.

# **Case Study: MIPS Processor**

## **Books Recommended**

- J. Hennessy & D. Patterson, Computer Architecture : A Quantitative Approach, Morgan Kaufmann Series, 5<sup>th</sup> Edition, 2011.
- Kai Hwang, Advance Computer Architecture: Parallelism, Scalability, Programmability, Mcgraw Hill Computer Science Series, 1992.
- D. Sima& T. Fountain & P. Kacsuk, Advance Computer Architectures : A Design Space Approach, 1<sup>st</sup> Edition, Pearson Education, 2002.
- J. Hayes, Computer Architecture and Organization, Mcgraw Hill Education Series (India), 2012.