

Institute of Engineering And Technology, DAVV
1 year VLSI

Sr No.	Roll Number	Enrollment Number	Student Name	ANALOG COMS CIRCUIT DESIGN	VERIFICATION & SYSTEM VERILOG	PHYSICAL VLSI DESIGN	DFT and Test & Testability	ANALOG CMOS CIRCUIT DESIGN	VERIFICATION & SYSTEM VERILOG	FPGA design using python	Result	SGPA
				2MVRC1	2MVRC2	2MVRC3	2MVRE3	2MVRL1	2MVRL2	2MVRO2		
				3	3	3	2	2	2	3		
				Th	Th	Th	Th	Pr	Pr	Th		
1	25MV2101	DE25969	AYUSH MAMORIYA	B	B+	A+	A	A	A	A+	Pass	7.83
2	25MV2102	DE25970	BHUMIKA KANNOJE	C	A	A+	A	A	A	A+	Pass	7.83
3	25MV2103	DE25971	PANKAJ VERMA	C	B+	A	A+	A	A	O	Pass	7.78
4	25MV2104	DE21353	PRANITA KALYANE	B	A	A+	A	A+	A+	Ab	Fail	6.72
5	25MV2105	DE25972	RAJNANDINI KUSHWAH	A	A	A+	A+	A	A	O	Pass	8.61
6	25MV2106	DE21261	SOUMYA BHARTI	B	A	A+	A+	A+	A+	O	Pass	8.5
7	25MV2107	DE25973	SUMEET CHAREL	B+	A	A+	A+	A+	A+	O	Pass	8.67
8	25MV2108	DE19274	VINIT GODALE	B	B+	A+	A+	A+	A+	O	Pass	8.33
No. of Failed Students				0	0	0	0	0	0	1		

Category	Number of Students
Pass	7
Fail	1
Not Registered	0



Dr. Hemant Makwana
Result Incharge
IET-DAVV, INDORE