| Devi Ahilya University, Indore, India<br>Institute of Engineering & Technology | | | | IVYear B.E. (Computer Engg.)<br>(Full Time) | | | |
|---|---|---|---|---|---|---|---|
| **Subject Code & Name** | **Instructions Hours per Week** | | | **Credits** | | | |
| **CER7E5** | **L** | **T** | **P** | **L** | **T** | **P** | **Total** |
| **VLSI Design** | **3** | **1** | **2** | **3** | **1** | **1** | **5** |
| **Duration of Theory Paper: 3 Hours** | | | | | | | |

**Course Objective:** This course presents the fundamental of Digital CMOS VLSI design with different VLSI design methodologies and combinational, sequential and semiconductor memory circuit design. It also covers the limitations of CMOS in NANO technology with introduction to the NANO Technology.

**Prerequisite:** Knowledge of Digital Circuit and Basics of Semiconductors is required.

## COURSE OF CONTENTS

**Unit I**

VLSI design flow, VLSI design style, introduction to the basic fabrication processes (wafer preparation, oxidation, diffusion, etching, metallization and lithography, etc.), Fabrication process Flow: basic Steps, the CMOS n-well Process. Metal oxide semiconductor (MOS) structure, Types of MOSFET: Enhancement and Depletion. Structure and operation of MOS transistor.

**Unit II**

Threshold voltage equation and energy band diagram of MOSFET, controlling of threshold voltage, MOSFET current – Voltage Characteristics. Transconductance, Drain conduction. Aspect ratio, process parameters, second order effects, MOS small signal and Large signal model, MOS capacitances. Stick diagram rules for nMOS and CMOS technology, lambda based and micron based design rules. Layout design for CMOS inverter

**Unit III**

Analysis of different types of inverter circuit, CMOS inverter, transfer characteristic, calculation of propagation delay, rise time, fall time, noise margin and power dissipation for CMOS Inverter. Effect of threshold voltage and supply voltage on Delay and power dissipation. Limitations of CMOS in NANO scale circuit design.

**Unit IV**

CMOS logic**,** Complex Logic Circuits, pseudo NMOS logic, pass transistor logic, Transmission Gate logic and Dynamic logic circuit design. Designing of Combinational logic circuit using CMOS and analysis of various design parameters.

**Unit V**

Sequential MOS Logic circuits , SR Latched circuits, clocked latch and Flip Flop Circuits, CMOS D latch and Edge Triggered Flip Flop, Design of the Schmitt trigger circuit, Dynamic random access and Static random access memory cell design and analysis, Sense amplifier and row and column decoder circuit.

**References:**

[1] Sung-mo Kang and Yusuf Leblebici, *CMOS Digital Integrated Circuit analysis and Design,*Tata McGraw-Hill, 3/e.

[2] R. Jacob Baker, Harry W. Li and David E. Boyce, *CMOS Circuit design, layout and Simulation*, PHI,IEEE press, Series Edition.

[3] Yuan Taur and Tak H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge university Press, Special Edition, 1998.

[4] Neil H.E. Weste and Kamran Esharhian, *Principal of CMOS VLSI design*, PHI, 2/e.

[5] Jan M. Rabaey, Digital Integrated Circuit, PHI, 2/e.