DIGITAL ELECTRONICS

Q.1 Design a 3 bit counter which counts in the sequence
: 001, 011, 010, 110, 111, 101, 001, ...
(a) Use clocked D flip-flops
(b) Use J-K flip-flop

Q.2 Design and Implement a 8-bit barrel shifter using 4 X 1 Multiplexers.

Q.3 Design a one-input, one-output serial 2's complementer. The circuit accepts a string of bits from the input and generates the 2's complement at the output. The circuit can be reset asynchronously to start and end the operation.

Q.4 Design a four-bit shift register with parallel load using D flip-flops. There are two control inputs: shift and load. When shift = 1, the content of the register is shifted by one position. New data are transferred into the register when load = 1 and shift= 0. If both control inputs are equal to 0, the content of the register does not change.

Q.5 Design a 16-bit Magnitude comparator using IC 7485 (4-bit Magnitude comparator).

Q.6 Design a hardware stack to hold a maximum of four values, each consisting of one bit. The stack has the following input lines:

- Clock
- POP
- PUSH
- input data

and a single output line. The output line always reports the current top of the stack. (Recall that a stack pushes data onto the top of the stack, and pops data from the top of the stack. In other words, last in, first out. If more than four values are pushed on, older values are discarded.)
You may use AND, OR, XOR, and NOT gates, etc; flip-flops of any kind; and/or decoders, multiplexers, etc.

ANALOG ELECTRONICS

Q.1 Design a common-emitter amplifier with output impedance 10KΩ and a gain of 100 using a transistor of β=200 and a 24V power supply.

Q.2 Design a two stage RC coupled BJT amplifier to meet the following specifications.
Av ≥ 5000, Sico ≤ 10,Fl = 20Hz, *Vo*=2*Vo*, Vcc = 15V.
Calaulate Av, Ri and Ro of designed circuit.

Q.3 Design a cascode amplifier stage using bipolar transistors to drive a load resistor of 100 Ω. The amplifier output is to be time varying signal of ±600mV. The overall performance of the amplifier is specified as:
• Operating current for cascade stage collectors = 1,2mA
• Overall gain = -30
• DC power supply +15V

Q. 4 Design the basic BJT differential amplifier to provide a differential input resistance of at and a differential voltage gain of 100 V/V. The transistor β is specified to be at least 100. The available positive power supply is 5V.

Q.5 Design a CMOS cascode amplifier with the following specifications:
DC gain = 2500
Gain-Bandwidth product = 100MHz.
Load capacitance = 1 pF

Q.6 Design a saw tooth generator using a 555 timer having a pulse duration of 10 sec and peak voltage of 5V.