Devi Ahilya University, Indore, India Institute of Engineering & Technology				**IV Year B.E. (Electronics and Telecommunication)**			
Subject Code & Name	**Instructions Hours per Week**			**Credits**			
ETR7E1	**L**	**T**	**P**	**L**	**T**	**P**	**Total**
CIRCUIT DESIGN USING HDL	**3**	**1**	**2**	**3**	**1**	**1**	**5**
Duration of Theory Paper: 3 Hours							

Learning Objective: To enable the students to translate a functional system description into appropriate digital blocks coded in VHDL.Perform synthesis, place, and route of a digital design into a target FPGA.

Prerequisite: Digital Design, C language.

COURSE CONTENTS

Unit I Introduction to VLSI and HDL

History of IC Design, IC Technology, Moore's Law, IC Design Constraints, Feature Size, VLSI Family, Programmable Logic Devices, Designing with Programmable Logic- Design Entry, Simulation, Synthesis, Implementation, Device Programming, EDA Tools, IP Cores, Gjeski's Y Chart.
Digital system design process, Hardware simulation, Levels of abstraction, VHDL requirements, Elements of VHDL Top down design, VHDL basic language Elements, VHDL operators, Timing, Concurrency, Objects and classes.

Unit II Behavioural Modeling

Signal assignments ,Concurrent and sequential assignments., Entity Declaration, Architecture Body, Behavioral Modeling, Process statement, Loop control statements, Multiple Processes, Delay Models, Signal Drivers.

Unit III Dataflow and Structural Modeling Techniques

Data flow Modeling, Concurrent Assignment statements, Block statements, Structural Modeling, Component declaration and Instantiation, Generate statements.

Unit IV Advance Topics in VHDL

Generics and Configuration, Subprogram, Overloading, Packages and Libraries, Design Libraries, Attributes.

Unit V Design for Synthesis

Language directed view of synthesis, Inference from CSA statements, Inference from within Process, Inference using Signals v/s variables, Latch v/s Flip Flop Inference, Wait statements, Synthesis Hints, Synthesis for dataflow and structural models.

Learning Outcomes:

At the end of the course, the students would be:

- Able to design digital systems through HDL language
- Simulation, synthesis and implementation of HDL code
- Implementation of code on FPGA/CPLD

BOOKS RECOMMENDED:

[1]. J. Bhasker, *VHDL* Primer, 3/e, Addison Wesley, 1999.
[2]. Sudhakar Yalamanchili, *Introductory VHDL-From Simulation to Synthesis*, Pearson Education, 3/e Indian Reprint.
[3]. Douglas Perry, *VHDL*, 3/e Edition, McGraw Hill 2001.
[4]. Peter.J.Ashenden, The Designer's Guide to *VHDL-AMS*,
[5]. Charles.H.Roth, *Digital system Design using VHDL*, Thompson Publishers, 2/e Edition, 2007.
[6]. Ben Cohen, *VHDL*-Coding style and Methodologies, Kluwer academic Publishers, 1995.
[7]. Volnei. A.Pedroni, *Circuit Design with VHDL*, *MIT* Press Cambridge, 2004.

List of Practical Assignments:

VHDL Programming using Xilinx ISE

Note: For Q1 to Q5 use behavioral modeling. For Q6 to Q7 use data flow modeling and for Q8 to Q10 use structural modeling.

Q.1 Write a VHDL code for a Full Adder.

Q.2 Write a VHDL code for 8X1 Multiplexer using if-elseif statement, case statement and nested if statement and compare their delay and area.

Q.3 Write a VHDL code for a 3X8 decoder using case statement.

Q.4 Write a VHDL code for a J-K flip-flop triggered at falling edge of clock pulse. Also include clear and reset pins synchronized with clock pulse.

Q.5 Write VHDL code for a synchronous 3-bit binary up-down counter. Include a selection line for selecting the mode of counting upwards or downwards.

Q.6 Design a combinational circuit with three inputs x, y, and z and three outputs A,B and C. when the binary input is 0,1,2, or 3 the binary output is one greater than the input otherwise the binary output is one less than the input.

Q.7 Write a VHDL code for a 3-bit binary code to 3-bit grey code conversion.

Q.8 Design a 4-bit ripple counter using T-Flip flop as basic component.

Q.9 Design a 4-bit Magnitude comparator using 1-bit Magnitude comparator as basic entity.

Q.10 Design a circuit of a 3-bit parity generator and the circuit of a 4-bit parity checker using an odd parity bit.