

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME – I Year (Spl Digital Communication) Semester- B				
Subject Code & Name		Instructions Hours per Week			Credits			
DCP4E1 Analog and Digital VLSI Circuit Design		L	T	P	L	T	P	Total
Duration of Theory Paper: 3 Hours		3	1	2	3	1	1	5

**Course Objectives:** This course presents the fundamental of CMOS VLSI design with different VLSI design methodologies and combinational, sequential and semiconductor memory circuit design. It also covers the limitations of CMOS in NANO technology with introduction to the NANO Technology.

**Prerequisite(s):** Knowledge of semiconductor devices is required.

### COURSE CONTENTS

#### UNIT -I

**Introduction:** VLSI design flow, VLSI design style, Fabrication process Flow: basic Steps, the CMOS n-well Process. Metal oxide semiconductor (MOS) structure, Types of MOSFET: Enhancement and Depletion. Structure and operation of MOS transistor. MOSFET process simulation.

#### UNIT -II

**MOS transistor:** threshold voltage of MOSFET, controlling of threshold voltage, MOSFET current – Voltage Characteristics. Transconductance, Drain conduction. Aspect ratio, process parameters, second order effects, MOS small signal and Large signal model, MOS capacitances.

#### UNIT -III

**CMOS Inverter:** Analysis of different types of inverter circuit, CMOS inverter, transfer characteristic, calculation of propagation delay, rise time, fall time, noise margin and power dissipation for CMOS Inverter. Effect of threshold voltage and supply voltage on Delay and power dissipation.

#### UNIT -IV

**CMOS circuit Design:** CMOS logic, pseudo NMOS logic, pass transistor logic, Transmission Gate logic and Dynamic logic circuit design. Designing of Combinational logic circuit, sequential logic circuit design and semiconductor memory circuit.

#### Unit –V

**CMOS Analog Circuit Design:** Large signal models, small signal models, current sources, single stage amplifiers, differential amplifiers, operational amplifiers, frequency response, frequency response of amplifiers, frequency response of operational amplifiers, stability and frequency compensation, frequency compensation

#### BOOKS RECOMMENDED

- [1]. Sung-mo Kang and Yusuf Leblebici, *CMOS Digital Integrated Circuit analysis and Design*, 3rd Edition, Tata McGraw-Hill.
- [2]. [Neil H.E. Weste and Kamran Esharhian, *Principal of CMOS VLSI design*, 2nd Edition, PHI, anded), AW/Pearson, 2001.
- [3]. CMOS mixed-signal circuit design by R. Jacob Baker Wiley India, IEEE press, reprint 2008.
- [4]. Design of analog CMOS integrated circuits by Behad Razavi McGraw-Hill, 2003.

**List of experiment:**

**Note : Use the BSIM3v3 (T-SPICE Level 49) model to characterize a 0.18 $\mu$ m CMOS process (TSMC).**

1. Determine the threshold voltage  $V_{TH}$  for the NMOS and PMOS devices (for  $V_{BS}=0$ ,  $L=0.18\mu\text{m}$  and  $W=1\mu\text{m}$ ), by extrapolating from the  $I_D-V_{GS}$  curve at low  $V_{DS}$ . Explain your circuit setup. How does this result compare to values reported in the model file? Also, determine the body-effect parameter.
2. Determine the subthreshold slope factor  $S$  for the NMOS and PMOS devices (at  $V_{DS}=1.8\text{V}$ , room temperature). Determine the leakage currents at  $V_{GS}=0\text{V}$ . Repeat it at a lower temperature  $T=77\text{K}$ .
3. Determine the effects of channel length  $L$  on the threshold voltage  $V_{Th}$  between  $0.18\mu\text{m}$  to  $2.0\mu\text{m}$ . Draw  $V_{Th}$  of the NMOS and PMOS as a function of  $L$  (for  $V_{DS}=1.8$  and  $1.2\text{V}$ ).
4. Determine the effects of drain-source voltage  $V_{DS}$ , on the threshold voltage  $V_{Th}$  between and  $1.8\text{V}$ . Draw  $V_{Th}$  as a function of  $V_{DS}$  (for  $L=0.18\mu\text{m}$ ). What is the measured DIBL factor?
5. With the given CMOS inverter Circuit calculate and estimate the static Characteristics
  - (a) Determine the VTC of CMOS Inverter
  - (b) Obtain the  $NM_H$ ,  $NM_L$ , and  $V_M$  for the inverter

## Dynamic Characteristics

- (c) Measure the  $t_{pHL}$ ,  $t_{pLH}$ ,  $t_p$ ,  $t_r$ ,  $t_f$
- (d) Power Consumption with varying load capacitances from  $100\text{fF}$  to  $500\text{fF}$ . And compute the power Delay Product (PDP) for the  $0.18\text{ Micron}$  technologies.