Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics (Sp. Digital Instrumentation) Semester- A			
Subject Code & Name	**Instructions Hours per Week**			**Credits**			
DIP1G1: Advance System Design	**L**	**T**	**P**	**L**	**T**	**P**	**Total**
Duration of Theory Paper: 3 Hours	**3**	**1**	**0**	**3**	**1**	**0**	**4**

Course Objective:

To provide an in-depth knowledge regarding designing of advance digital system. To emphasizeon system design for timing and performance trade off.

Prerequisite:

Knowledge of basic digital electronics, state diagrams and graph theory.

COURSE CONTENTS

Unit I

Introduction to digital IC design – full Custom and semi-custom design flow and comparison,
Combinational Logic Design, Synchronous State Machine Design and Analysis, Asynchronous State Machine Design and Analysis, Synthesis and Optimization of Digital Circuit (AREA, POWER AND DELAY). LOW and High Level Synthesis process, optimization of hardware. combinational logic synthesis – Technology independent and technology dependent optimization –Logic synthesis

Unit II

High level synthesis- Scheduling and allocation-ASAP and ALAP scheduling-Register allocation-Functional Unit allocation-Interconnect path allocation-Hardware description languages-synthesis-register transfer design-Event driven simulation. Low power issues in high level synthesis and logic synthesis.

Unit III

Resource Sharing and Binding, Sharing and Binding for Resource-Dominated Circuits, Resource Sharing in Non-Hierarchical Sequencing Graphs, Resource Sharing in Hierarchical Sequencing Graphs, Register Sharing, Multi-Port Memory Binding, Bus Sharing and Binding, Sharing and Binding for General Circuits, Unconstrained Minimum-Area Binding.

Unit IV

Subsystem design principles pipelining - Data paths in processor architecture – Standard cell design considerations of adder and multiplier- Timing -Slack delay model – Effect of skew and jitter on timing, Sources of skew and jitter- Clocking disciplines -Wire model- Technology scaling effect on interconnect and - Noise in interconnects.

Unit V

FPGAs Introduction to FPGA, FPGA Programming technologies, Static SRAM, Anti Fuse, EPROM, EEPROM, Xilinx FPGA (XC2000, XC3000, XC4000 and XC5000), Logic block Architecture. Field Programmable Logic Sequencer, application of FPLS Devices. Programmable Array Logic Series 20, Combinational PAL Devices, Sequential PAL Devices, Arithmetic PAL Devices.

Text and Reference Books:

[1] John M Yarbrough, “Digital Logic Applications and Design”, Thomson learning
[2] Synthesis and optimization of Digital Circuits , Giovanni De Micheli , Tata Mc Graw Hill Edition
[3] Jan M Rabaey, Digital Integrated Circuits - A Design Perspective, Prentice Hall, Second Edition, 2005.
[4] Naveed A. Sherwani, Algorithms for VLSI Physical Design Automation, Springer,Third edition,1999.