

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics (Sp. Digital Instrumentation) Semester- B			
Subject Code & Name	Instructions Hours per Week			Credits			
DIR2C3: System Design using Verilog	L	T	P	L	T	P	Total
Duration of Theory Paper: 3 Hours	3	1	2	3	1	1	5

Course Objectives:

To enable the students to translate a functional system description into appropriate digital blocks coded in Verilog. Perform synthesis, place, and route of a digital design into a target FPGA

Prerequisite(s):

Digital Design, Microprocessor architecture, C++ language.

COURSE CONTENTS

Unit I

Overview of Digital Design with Verilog HDL: Evolution of CAD, emergence of HDLs, typical HDL-based design flow, why Verilog HDL?, trends in HDLs.

Hierarchical Modeling Concepts: Top-down and bottom-up design methodology, differences between modules and module instances, parts of a simulation, design block, stimulus block.

Basic Concepts: Lexical conventions, data types, system tasks, compiler directives.

Unit II

Modules and Ports: Module definition, port declaration, connecting ports, hierarchical name referencing.

Gate-Level Modeling: Modeling using basic Verilog gate primitives, description of andlor and buflnotttype gates, rise, fall and turn-off delays, min, max, and typical delays.

Dataflow Modeling: Continuous assignments, delay specification, expressions, operators, operands, operator types.

Unit III

Behavioral Modeling: Structured procedures, initial and always,blocking'and nonblocking statements, delay control, event control, conditional statements, multiway branching, loops, sequential and parallel blocks.

Tasks and Functions -Differences between tasks and functions, declaration, invocation.

Useful Modeling Techniques: Procedural continuous assignments, overriding parameters, conditional compilation and execution, useful system tasks.

Unit IV

Timing and Delays: Distributed, lumped and pin-to-pin delays, specify blocks, parallel and full connection, timing checks, delay back-annotation.

Switch-Level Modeling: MOS and CMOS switches, bidirectional switches, modeling of power and ground, resistive switches, delay specification on switches.

Unit-V

Logic Synthesis with Verilog HDL: Introduction to logic synthesis, impact of logic synthesis, Verilog HDL constructs and operators for logic synthesis, synthesis design flow, verification of synthesized circuits, modeling tips, design partitioning.

Text Books and References:

- [1] Samir Palnitkar , “Verilog HDL-A guige to Digital Design and Synthesis “ 2nd Edition, Pearson , 2006.
- [2] J. Bhaskar, “A Verilog HDL Primer”, B.S Publications,
- [3]Douglas J. Smith, “Hdl Chip Design : A Practical Guide for Designing, Synthesizing & Simulating ASICs &FPGAs Using VHDL or Verilog”.Doone Pubns ,1998.
- [4] Blaine Readler , “Verilog by Example: A Concise Introduction for FPGA Design”, Full Arc Press, 2011