Devi Ahilya University, Indore, India Institute of Engineering & Technology				MSc – I Year (Applied Mathematics) with Specialization in Computing & Informatics Semester- I			
Subject Code & Name	**Instructions Hours per Week**			**Credits**			
AM1GE1: Computer Architecture/ Digital Electronics & Computer Organization	**L**	**T**	**P**	**L**	**T**	**P**	**Total**
	3	**1**	**-**	**3**	**1**	**-**	**4**
Duration of Theory Paper: 3 Hours							

Objective: Aim of this course is to aware students about the hardware of computers, get acquainted with different number systems, their Inter-conversion and operations. Familiarized with different logic families & relative performance Ability to design various combinational circuits by solving & reducing Boolean equations, Familiarize with the internal working of modern computer systems
Prerequisite(s): Computer Programming

COURSE OF CONTENTS

UNIT-I
Introduction to Computer Architecture, Memory Organization and Control Design: Introduction, CPU Organization, Instruction Sets, Memory Technology, Memory system, Caches, Basic concepts of control design, micro programmed Control and Pipeline Control.

UNIT II
Binary Systems: Digital Systems, Binary Numbers, Binary Codes, Error detecting Code. Computer Arithmetic Number Base Conversions, Octal and Hexadecimal – conversions. Boolean Algebra and Logic Gates, Functions Minterms and Maxterms – Laws and theorems of Boolean Algebra – Demorgan's theorems – The Universal Building blocks – NAND & NOR gates as universal Building Blocks.

UNIT III
Simplification of Boolean Expressions : Canonical SOP and POS forms – Algebraic Simplification – Karnaugh Maps – SOP & POS Simplification – NAND / NOR implementation of Boolean expressions – Don't care, conditions – Overlapping groups, eliminating redundant groups. Combinational Logic circuits : Half and Full Adders – Half and Full subtractors – BCD adder – parallel binary adder – Multiplexer & Demultiplexer – Encoder & Decoder.

UNIT IV
Sequential Logic circuits: NAND latch – SR, flipflop – JK flipflop – Edge triggering – PRESET and CLEAR inputs, Shift Register, Universal Shift register – Asynchronous and Synchronous counters – BCD counter.

UNIT V
Parallel Computer Models: Introduction - Flynn's Classifications - Parallel & Vector Computer System - Attributes to performance - implicit and explicit parallelism - shared memory – multiprocessors – Uniform and Non-Uniform Memory Access and Cache only Memory Access Models – Distributed Memory Multicomputers – Multivector & SIMD Computers – PRAM and VLSI Module

BOOKS RECOMMENDED:
[1] John P. Hayes, Computer Architecture and Organization, McGraw Hill, 3rd Ed., 1998.
[2] Kai Hwang, Advanced Computer Architecture, McGraw Hill, 1993.
[3] Stallings W., Computer Organization and Architecture, Designing for Performance, Prentice Hall, 2010.

[4] Meena K, Principles of Digital Electronics, PHI Learning Pvt. Ltd., 2009
[5] Thomas Bartee C, Digital Computer Fundamentals, TMH, 6th Edition, 1995.
[6] Moris Mano, Computer Architecture and Logic Design, TMH Publications, ND, 2002.
[7] Nicholas Carter, Computer Architecture Schaum Series Adaptation, 2nd edition, 2011.