Devi Ahilya University, Indore, India Institute of Engineering & Technology				**II Year B.E. (Electronics and Telecommunication Engg.)**			
Subject Code & Name	**Instructions Hours per Week**			**Credits**			
3ETRC2	**L**	**T**	**P**	**L**	**T**	**P**	**Total**
DIGITAL ELECTRONICS	**3**	**1**	**2**	**3**	**1**	**1**	**5**
Duration of Theory Paper: 3 Hours							

Learning Objectives:

- Provide student the knowledge of different number systems and conversion among them.
- Familiarize students with different logic families and characteristics of Digital ICs
- Develop skills to design different Combinational circuits.
- Develop skills to design various Sequential circuits
- Develop ability to implement digital circuits through VHDL and Programmable logic devices (PLDs).

Prerequisites:

Knowledge of Transistor, Diodes, Switching property, Boolean algebra.

COURSE CONTENTS

Unit –I

Foundation: Number system, Arithmetic operations using 1's,2's complement, various codes, Review of basic gates, universal gate application, Logic Families: - RTL, DTL, TTL & MOS, CMOS families for NOR/NAND gate, characteristics of Digital IC's- speed of operation, power dissipation, Fan-in, Fan-out, Noise margin, Current and Voltage parameters, Moore's Law, IC Design Constraints, Feature Size .

Unit-II

Combinational Circuits: Boolean laws & algebra , Sum Of Product & Product Of Sum expression, K-Map and Tabular method of minimization, Ccombinational devices like Multiplexer, Demultiplexer, Decoders, Encoders, Combinational circuit design for Adder, Subtractor, Comparator, Multiplier ,Code converters

Unit-III

Sequential Circuits: Latches and Flip-Flop- SR, D, T, JK, Master-slave , Flip- Flop conversions, Counter and Registers**:** Synchronous counter, Asynchronous counter, Up-Down Counter, Shift Registers -serial in parallel out, serial in serial out, parallel in serial out, parallel in parallel out, Universal Shift Register

Unit-IV
Digital to Analog Conversion Technique as Binary Weighted DAC, R-2R Ladder, Analog to Digital Conversions as Flash type, Counter type, Successive Approximations type A/D converter, Specifications of A/D converters.

Unit-V
VLSI Family, Programmable Logic Devices, Designing with Programmable Logic- Design Entry, Simulation, Synthesis, Implementation, Device Programming,
Introduction to VHDL: VHDL basic language Elements, VHDL operators, Objects and classes. Behavioral Modeling-- Signal assignments ,Concurrent and sequential assignments., Entity Declaration, Architecture Body, Process statement, Loop control statements, Data flow Modeling, Concurrent Assignment statements, Structural Modeling, Component declaration and Instantiation, Generate statements

Learning Outcomes:

Upon completing the course, students will be able to:

- Understand driving capacity of a gate and voltage-current parameters.
- Implement digital circuit for arithmetic operations.
- Implement digital circuit with optimized hardware.
- Design and Analyse any combinational digital circuit
- Design and Analyse any sequential circuit
- Using analog to digital and digital to analog IC's for data conversion.
- Design circuit to generate clock and pulses of desired frequency.
- Design Combinational and sequential circuits through VHDL and implement on PLDs.

BOOKS RECOMMENDED:

[1] Mano M. Morris, "*Digital Design*", 3rd edition, Pearson Education 2006.
[2] William H.Gothmann,"*Digital Electronics: An Introduction to Theory and Practice,* Eastern Economy Edition , Prentice-Hall of India Private Limited,NewDelhi.,2001
[3] William I. Fletcher, "*An Engineering Approach to Digital Design"*, Pearson Education
[4] S Salivahan, SArivazhagan *"Digital Circuit and Design*" Vikas Publication , 2013
[5] J. Bhasker, *VHDL* Primer, 3/e, Addison Wesley, 1999.

List of Practical Assignments:

Designing of basic combinational and sequential circuits on breadboard using IC's.

VHDL Programming using Xilinx ISE/Vivado

Note: For Q1 to Q5 use behavioral modeling. For Q6 to Q7 use data flow modeling and for Q8 to Q10 use structural modeling.

Q.1 Write a VHDL code for a Full Adder.

Q.2 Write a VHDL code for 8X1 Multiplexer using if-elseif statement, case statement and nested if statement and compare their delay and area.

Q.3 Write a VHDL code for a 3X8 decoder using case statement.

Q.4 Write a VHDL code for a J-K flip-flop triggered at falling edge of clock pulse. Also include clear and reset pins synchronized with clock pulse.

Q.5 Write VHDL code for a synchronous 3-bit binary up-down counter. Include a selection line for selecting the mode of counting upwards or downwards.

Q.6 Design a combinational circuit with three inputs x, y, and z and three outputs A,B and C. when the binary input is 0,1,2, or 3 the binary output is one greater than the input otherwise the binary output is one less than the input.

Q.7 Write a VHDL code for a 3-bit binary code to 3-bit grey code conversion.

Q.8 Design a 4-bit ripple counter using T-Flip flop as basic component.

Q.9 Design a 4-bit Magnitude comparator using 1-bit Magnitude comparator as basic entity.

Q.10 Design a circuit of a 3-bit parity generator and the circuit of a 4-bit parity checker using an odd parity bit.