<table>
<tr><td colspan="5">Devi Ahilya Vishwavidhyalaya, Indore, India
Institute of Engineering & Technology</td><td colspan="2">II Year B.Tech.
(Computer Science and Engineering)</td></tr>
<tr><td>Course Code & Name</td><td colspan="6">Instructions Hours per Semester and Credits</td></tr>
<tr><td rowspan="3">3RCPC4
Digital Logic and Computer Organization</td><td colspan="2">Classroom Instruction (CI)</td><td>Lab Instruction (LI)</td><td>Term Work (TW) and Self Learning (SL)</td><td>Total no. of Hours Per semester</td><td>Total Credits (Total Hours/30)</td></tr>
<tr><td>L</td><td>T</td><td>P</td><td>TW+SL</td><td rowspan="2">90</td><td rowspan="2">3</td></tr>
<tr><td>30</td><td>10</td><td>0</td><td>50</td></tr>
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Learning Objectives:

1. To introduce students to ideas and techniques from digital logic and computer organization that concept are widely used in Computer Science.
2. To understand the concepts of computer organization and architecture, Register transfer, types of memory and memory hierarchy.
3. To understand the logic gates, Boolean algebra and its theorems.
4. To understand the concept of pipeline.

Prerequisites: Knowledge of Computer organization, Digital logic and circuits.

COURSE CONTENTS

Unit-I

Historical perspective: Generation of computer, Evolution of computer, Types of Computer.
Basic operational concepts: Difference between computer organization and computer architecture, Flynn classification, Functional units, Multiprocessors and microcomputers, Bus structure and Common bus system, Instruction cycle, John Neumann Architecture, Addressing modes
Software performance: Processor Clock, Clock rate, Basic performance equation, compiler performance measurement.
Arithmetic for computers: Addition, subtraction and multiplication of signed numbers, Booth Algorithm.

Unit-II

Digital Logic: Logic gates and logic expressions, Boolean algebra: Laws and theorems
Minimization: Karnaugh map, Quine – McClusky method
Number system: binary, octal, decimal and hexadecimal number representation and conversion
.

Unit-III

Design and Analysis of combinational circuit: adders, subtractors, multiplexers, decoders.
Sequential circuits: Flip- flops, latches, counters, registers.

Unit-IV

Memory Hierarchy: Hierarchy structure of memory, RAM, ROM, Flash memory: Memory speed, size and cost considerations.
Cache Memories: Cache concept, mapping function, Replacement algorithm, Hit rate and miss penalty, Cache on processor chip, virtual memories. .
I/O organization: Program driven I/O, Interrupt driven I/O, Direct memory access.

Unit-V

ALU: Design and operation of ALU**.**

Data Path: Data path and control unit(Hardwired and micro programmed).

Pipeline: Instruction pipeline stage and implementation, principles of pipeline and linear pipeline, clock period, speed up, efficiency, throughput, classification of pipeline processor, general pipelines and reservation tables, collision vector, state diagram for a pipeline, pipeline hazards: data control, structural, mitigation techniques.

Course Outcome (CO):

CO. No.	CO
CO1	Understand the historical evolution and classification of computers, distinguish between computer organization and architecture, Analyse instruction cycles, understand processor architecture including John, Neumann model, addressing modes, data path design, identify the different computer types and system structures and evaluate basic operational concepts including processor performance and arithmetic operations in digital system.
CO2	Understand and apply the principles of digital logic design, number system, representations, and logic minimization techniques.
CO3	Understand and implement the combinational circuit and sequential circuit design.
CO4	Describe the memory hierarchy, cache memory concepts, virtual memory concepts, virtual memory and understand input/ output(I/O) organization techniques.
CO5	Understand the design and functioning of the arithmetic Logic unit (ALU), explain data path control and analyse instruction pipeline techniques and associated hazards.

Books Recommended:

[1]. M.Morris Mano, Computer system Architecture,3rd Edition, Pearson Education, 2007
[2]. William Stallings, Computer organization and Architecture,10th edition Pearson Education 2016.
[3]. Brian Holdsworth Digital Logic Design, 4thEdition
[4]. M. Morris Mano , Digital Logic and Computer Organization, Pearson Education, India, 2017

CO-PO- PSO Relationship:

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
3RCPC4.CO1	3	3	2	2	-	1						2	3	2
3RCPC4.CO2	3	3	2	2	-							2	3	2
3RCPC4.CO3	3	3	3	2	-							2	3	2
3RCPC4.CO4	3	3	-	2	-							2	3	2
3RCPC4.CO5	3	2	-	-	3							2	3	3