<table>
<tr><td colspan="5">Devi Ahilya Vishwavidhyalaya, Indore, India
Institute of Engineering & Technology</td><td colspan="2">II Year B.Tech. (Electronics and Telecommunication Engineering)</td></tr>
<tr><td>Course Code & Name</td><td colspan="6">Instructions Hours per Semester and Credits</td></tr>
<tr><td rowspan="2">4RTPC1

COMPUTER ARCHITECTURE AND DIGITAL DESIGN</td><td colspan="2">Classroom Instruction (CI)</td><td>Lab Instruction (LI)</td><td>Term Work (TW) and Self Learning (SL)</td><td>Total no. of Hours Per semester</td><td>Total Credits (Total Hours/30)</td></tr>
<tr><td>L</td><td>T</td><td>P</td><td>TW+SL</td><td rowspan="2">90</td><td rowspan="2">3</td></tr>
<tr><td>20</td><td>10</td><td>0</td><td>60</td></tr>
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Course Learning Objectives:

1. To develop in-depth understanding of advanced digital design concepts.
2. To analyze sequential and control-oriented digital systems.
3. To explain processor organization and datapath design.
4. To understand memory hierarchy and performance enhancement techniques.
5. To evaluate computer system performance using architectural metrics.

Prerequisite:

Digital Electronics, Basic Computer Organization

COURSE CONTENTS

UNIT I Advanced Combinational Digital Design

Review of combinational logic design, timing analysis, propagation delay, setup and hold time, advanced arithmetic circuits such as carry look-ahead, carry select adders, comparators, encoders, decoders, and ALU design principles.

UNIT II: Advanced Sequential Digital Design

Sequential building blocks, registers and shift registers, synchronous and asynchronous counters, sequence generators and detectors, clocking strategies, synchronization and metastability.

UNIT III: Control-Oriented Digital Design

Finite State Machines (Moore and Mealy models), state minimization and assignment, Algorithmic State Machine (ASM) charts, hardwired control unit design, datapath and control separation.

UNIT IV: Processor Organization and Datapath

Computer organization vs architecture, instruction cycle, instruction formats, addressing modes, single-cycle and multi-cycle datapath design, control signals and instruction execution.

UNIT V: Memory, I/O and Performance Analysis

Memory hierarchy, cache mapping techniques and policies, virtual memory concepts, programmed I/O, interrupt-driven I/O, DMA, bus architectures, performance metrics (CPI, throughput, latency), Amdahl’s Law, overview of multicore processors.

Course Outcomes:

CO.No.	CO
CO1	Students will be able to analyze and design advanced combinational digital circuits by applying timing analysis concepts such as propagation delay, setup and hold time, and by designing high-performance arithmetic blocks including carry look-ahead and carry select adders, comparators, encoders, and arithmetic logic units (ALUs).
CO2	Students will be able to design and analyze sequential digital systems using registers, shift registers, counters, and sequence generators, and will understand clocking strategies, synchronization issues, and metastability in complex digital systems
CO3	Students will be able to model and analyze control logic for digital systems using Moore and Mealy finite state machines, apply state minimization and assignment techniques, develop Algorithmic State Machine (ASM) charts, and explain the design of hardwired control units and datapath–control separation
CO4	Students will be able to explain and analyze processor organization and datapath design, including instruction cycles, instruction formats, addressing modes, and the operation of single-cycle and multi-cycle processors with appropriate control signal sequencing
CO5	Students will be able to analyze memory hierarchy and input–output organization and evaluate overall processor performance using metrics such as CPI, throughput, and latency, apply Amdahl's Law for performance estimation, and understand the architectural concepts of modern multicore processors

Books Recommended:

[1]. Harris & Harris – Digital Design and Computer Architecture, Morgan Kaufmann.
[2]. Patterson & Hennessy – Computer Organization and Design, Morgan Kaufmann.
[3]. M. Morris Mano – Digital Logic and Computer Design, Pearson.

CO-PO-PSO Relationship

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO 1	PSO 2	PSO 3
4RTPC1 .CO1	3	3	2									3	2	1
4RTPC1.CO2	3	3	2									3	2	1
4RTPC1.CO3	3	3	3								2	3	3	2
4RTPC1.CO4	3	3	2	-	2						2	3	3	2
4RTPC1.CO5	3	3	-	2	2						3	3	3	3