Devi Ahilya University, Indore, India Institute of Engineering & Technology				**III Year B.E. (Electronics and Instrumentation)**			
Subject Code & Name	**Instructions Hours per Week**			**Credits**			
5EIRC1	**L**	**T**	**P**	**L**	**T**	**P**	**Total**
SOC DESIGN USING HDL	**3**	**1**	**0**	**3**	**1**	**0**	**4**
Duration of Theory Paper: 3 Hours							

Course Objective:

The course is designed

1. To understand the basics of VLSI Design Methodologies.
2. To understand the Concept of PLD based VLSI Design on FPGA/CPLD.
3. To apply the concept of Digital design for designing basic logic cells using Verilog HDL.
4. To implement various Digital circuit/Modules through different Verilog Modelling Techniques.
5. To Understand the concept of Simulation, Synthesis and Implementation of Digital design on PLD through EDA Tool

COURSE CONTENTS

Unit 1

Implementation Strategies for Digital ICs: Introduction to Hardware Design: Digital System Design Process, Hardware Description Languages, Hardware Simulation, Hardware Synthesis, Levels of Abstraction.

Unit 2

Resistive, Capacitive and Inductive Parasitic: Timing Parameter Definition – Setup Timing Check- Hold Timing Check- Multicycle Paths- False Paths - Clocking of Synchronous Circuits. timing classification of digital systems - Synchronous Design - Origins of Clock Skew/Jitter and impact on Performance - Clock Distribution Techniques - Latch based clocking - Clocking tree topologies: H-tree, X-tree. Elmore delay model to calculate skew- Buffer insertion in clock trees- Exact Zero skew clock routing algorithm.

Unit 3

Verilog HDL: Introduction to Verilog HDL, Abstraction levels, basic concepts, Verilog primitives, keywords, data types, nets and registers, Verilog Modules and ports,Verilog OperatorsTheory Logical Operators, Bitwise and Reduction Operators, Concatenation and Conditional Operators, Relational and Arithmetic, Shift and Equality Operators, Operator Execution Order. Assignments: Types of Assignments, Continuous Assignment, Procedural Assignments, Blocking and Non-Blocking Assignments, Tasks and Functions

Unit 4 :

Verilog Modelling: Theory Gate Type, Design Hierarchy, Gate Delay, Propagation Delay, Logic Simulation Dataflow-Level Modelling: Assignments, Behavioural Modeling: Always Block, Flow Control, If-Else, Case, Cases, While Loop, For Loop, Repeat

Unit 5:
FPGA Architecture and Design: Introduction to Xilinx EDA Tool. Introduction with XST Tool and ISIM Tool Xilinx Tool Flow: Simulation and Synthesis, Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects Programmable I/O Blocks in FPGAs, Dedicated Specialized Components of FPGAs, Device Architecture Xilinx Spartan VI and zynq-7000 Architectures.

Course Outcome:

Students earned credits will develop ability to

CO.No.	CO	PO
CO1	Design and model combinational circuits with Verilog HDL at different levels.	PO-1,PO-2
CO2	Design and analyse various sequential digital circuits by Verilog HDL	PO-1,PO-2
CO3	Understand the different Modelling styles, Functions ,Tasks and advance designing for PLD	PO-1, PO-2, PO-3, PO-5
CO4	Analyse different types of FPGAs and their modules	PO-1, PO-2, PO-3, PO-5
CO5	Understand the Project/Module Design using Xilinx FPGA board	PO-1, PO-2, PO-3, PO-5

CO-PO Relationship

CO	PO-1	PO-2	PO-3	PO-4	PO-5	PO-6	PO-7	PO-8	PO-9	PO-10	PO-11	PO-12
CO1	3	3										
CO2	2	2	1									
CO3	2	2	1		2							
CO4	2	2	1		2							
CO5	2	2	1		2							

BOOKS RECOMMENDED:

[1]. Rabaey, Jan M. Digital integrated circuits a design perspective
[2]. Palnitkar, Samir. “Verilog HDL: A Guide To Digital Design and Synthesis”, Pearson Education India,
[3]. Navabi, Zainalabedin, and Yuwen Xia. “Verilog Digital System Design: Register Transfer Level Synthesis, Testbench, and Verification”, McGraw-Hill
[4]. Bhasker, Jayaram “Verilog HDL Synthesis: A Practical Primer”, Star Galaxy Publishing
[5]. Wolf, Wayne. FPGA-Based System Design”. Pearson education