Devi Ahilya Vishwavidhyalaya, Indore, India Institute of Engineering & Technology						III Year B.Tech. (Electronics and Telecommunication Engineering)
Course Code & Name	**Instructions Hours per Semester and Credits**					
5RTPE1 **CMOS Digital VLSI Design and Fabrication**	**Classroom Instruction (CI)**		**Lab Instruction (LI)**	**Term Work (TW) and Self Learning (SL)**	**Total no. of Hours Per semester**	**Total Credits (Total Hours/30)**
	L	**T**	**P**	**TW+SL**	**120**	**4**
	20	**10**	**20**	**70**		

Course Learning Objectives:

1. Understand semiconductor physics and MOS device operation.
2. Analyze CMOS inverter characteristics, delay, power and noise margins.
3. Design CMOS combinational and sequential logic circuits.
4. Understand CMOS fabrication processes and layout concepts.
5. Develop practical skills in CMOS design using CAD tools and fabrication flow.

Prerequisites:

Knowledge of Digital Electronics, Transistor, Diodes.

COURSE CONTENTS

Unit-I

Semiconductor fundamentals, intrinsic/extrinsic semiconductors, PN junction, MOS capacitor, energy bands, channel formation, enhancement/depletion MOSFET, NMOS/PMOS characteristics, threshold voltage, body effect, MOS capacitances.

Unit-II

CMOS technology, CMOS inverter, resistive/enhancement/depletion load inverters, voltage transfer characteristics, switching threshold, static and dynamic behavior, small signal model, propagation delay, power dissipation.

Unit-III

CMOS logic design: Static CMOS, ratioed logic, pass transistor logic, transmission gate logic, dynamic CMOS, domino logic, clocked CMOS, logic effort, delay optimization, stick diagrams, lambda-based design rules.

Unit-IV

Pass Transistor Logic, Pseudo NMOS Logic, Transmission Gate Logic, Dynamic CMOS Logic, Domino logic, Clocked CMOS Logic, Logic Effort, Delay Optimization, Comparison of CMOS Logic Families,

Unit-V

Introduction to CMOS Fabrication , Silicon Wafer Preparation, Oxidation, Photolithography, Diffusion, Ion Implantation, Epitaxy, Thin Film Deposition, Etching, Metallization, N-Well,

P-Well and Twin-Tub Processes, Design Rules, Latch-up, Packaging and Testing, Overview of Modern CMOS Technologies

CO.No.	CO
CO1	Explain semiconductor physics and MOS transistor operation.
CO2	Analyze CMOS inverter characteristics, delay, power and noise
CO3	Design CMOS logic circuits using different logic styles.
CO4	Design, evaluation and comparison of various CMOS based logic families.
CO5	To learn the Basic Fabrication and packaging process.

Books Recommended:

[1]. Neil H. E. Weste & David Harris, CMOS VLSI Design.
[2]. Jan M. Rabaey, Digital Integrated Circuits.
[3]. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits.
[4]. Stephen Campbell, Fabrication Engineering at the Micro and Nanoscale.
[5]. S. M. Sze & Kwok K. Ng, Physics of Semiconductor Devices.
[6]. John P. Uyemura, Introduction to VLSI Circuits and Systems.

CO-PO-PSO Relationship

CO	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PSO 1	PSO 2	PSO 3
CO 1	3	3	2	1								3	2	1
CO 2	3	3	3	2	2							3	3	2
CO 3	3	3	3	3	3							3	3	3
CO 4	3	3	3	3	3					1		2	3	3
CO 5	3	2	3	3	3	1	2			1	1	2	3	3

List of Practical Assignments (Cadence Virtuoso / Tanner EDA)

1. Installation and familiarization of Tanner EDA/Cadence Virtuoso environment.
2. DC analysis of NMOS and PMOS transistors and extraction of I–V characteristics.
3. Design and simulation of CMOS Inverter; obtain VTC, noise margin and switching threshold.
4. Transient analysis of CMOS Inverter to determine propagation delay, rise/fall time and power dissipation.
5. Design and simulation of CMOS NAND and NOR gates.
6. Design of XOR/XNOR gate using Transmission Gate Logic.
7. Implementation of Pass Transistor Logic and comparison with Static CMOS.
8. Design and simulation of Dynamic CMOS and Domino Logic circuits.
9. CMOS layout design of Inverter and NAND gate using Cadence Virtuoso/Tanner L-Edit.
10. Perform Design Rule Check (DRC), Layout Versus Schematic (LVS) and parasitic extraction.
11. Design, layout and simulation of a 1-bit Full Adder in CMOS.

12. Mini Project: Design, layout and verification of a small digital subsystem (4-bit Ripple Carry Adder / 4×1 Multiplexer / Decoder) using Cadence or Tanner.