

Devi Ahilya Vishwavidhyalaya, Indore, India Institute of Engineering & Technology					III Year B.Tech. (Electronics and Telecommunication Engineering)	
Course Code & Name	Instructions Hours per Semester and Credits					
5RTPE1 CMOS DIGITAL VLSI DESIGN AND FABRICATION	Classroom Instruction (CI)		Lab Instruction (LI)	Term Work (TW) and Self Learning (SL)	Total no. of Hours Per semester	Total Credits (Total Hours/3 0)
	L	T	P	TW+SL	120	4
	20	10	20	70		

Course Learning Objectives:

1. Understand semiconductor physics and MOS device operation.
2. Analyze CMOS inverter characteristics, delay, power and noise margins.
3. Design CMOS Combinational and Sequential logic circuits.
4. Understand CMOS fabrication processes and layout concepts.
5. Develop practical skills in CMOS design using CAD tools and fabrication flow.

Prerequisites:

Knowledge of Digital Electronics, Transistor, Diodes.

COURSE CONTENTS

Unit-I

Semiconductor fundamentals, intrinsic/extrinsic semiconductors, PN junction, MOS capacitor, energy bands, channel formation, enhancement/depletion MOSFET, NMOS/PMOS characteristics, threshold voltage, body effect, MOS capacitances.

Unit-II

CMOS technology, CMOS inverter, resistive/enhancement/depletion load inverters, voltage transfer characteristics, switching threshold, static and dynamic behavior, small signal model, propagation delay, power dissipation.

Unit-III

CMOS logic design: Static CMOS, ratioed logic, pass transistor logic, transmission gate logic, dynamic CMOS, domino logic, clocked CMOS, logic effort, delay optimization, stick diagrams, lambda-based design rules.

Unit-IV

CMOS Fabrication: Silicon wafer, oxidation, photo-lithography, diffusion, ion implantation, epitaxy, deposition, etching, metallization, N-well, P-well, twin-tub process, latch-up, packaging, testing.

Unit-V

CMOS layout and VLSI design flow, layout versus schematic (LVS), design rule check (DRC), parasitics, introduction to Cadence/Synopsys tools, overview of FinFET and advanced CMOS technologies.

CO.No.	CO
CO1	Explain semiconductor physics and MOS transistor operation.
CO2	Analyze CMOS inverter characteristics, delay, power and noise
CO3	Design CMOS logic circuits using different logic styles.
CO4	Explain CMOS fabrication technology and layout rules.
CO5	Apply CMOS VLSI design flow using modern EDA tools.

Books Recommended:

- [1]. Neil H. E. Weste & David Harris, CMOS VLSI Design.
- [2]. Jan M. Rabaey, Digital Integrated Circuits.
- [3]. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits.
- [4]. Stephen Campbell, Fabrication Engineering at the Micro and Nanoscale.
- [5]. S. M. Sze & Kwok K. Ng, Physics of Semiconductor Devices.
- [6]. John P. Uyemura, Introduction to VLSI Circuits and Systems.

CO-PO-PSO Relationship

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO 1	PSO 2	PSO 3
5RTPE1.CO1	3	3	2	1								3	2	1
5RTPE1.CO2	3	3	3	2	2							3	3	2
5RTPE1.CO3	3	3	3	3	3							3	3	3
5RTPE1.CO4	3	2	2	3	2							3	2	3
5RTPE1.CO5	3	3	3	3	3				1	2	1	3	3	3

List of Practical Assignments (Cadence Virtuoso / Tanner EDA)

1. Installation and familiarization of Tanner EDA/Cadence Virtuoso environment.
2. DC analysis of NMOS and PMOS transistors and extraction of I–V characteristics.
3. Design and simulation of CMOS Inverter; obtain VTC, noise margin and switching threshold.
4. Transient analysis of CMOS Inverter to determine propagation delay, rise/fall time and power dissipation.
5. Design and simulation of CMOS NAND and NOR gates.
6. Design of XOR/XNOR gate using Transmission Gate Logic.

7. Implementation of Pass Transistor Logic and comparison with Static CMOS.
8. Design and simulation of Dynamic CMOS and Domino Logic circuits.
9. CMOS layout design of Inverter and NAND gate using Cadence Virtuoso/Tanner L-Edit.
10. Perform Design Rule Check (DRC), Layout Versus Schematic (LVS) and parasitic extraction.
11. Design, layout and simulation of a 1-bit Full Adder in CMOS.
12. Mini Project: Design, layout and verification of a small digital subsystem (4-bit Ripple Carry Adder / 4×1 Multiplexer / Decoder) using Cadence or Tanner.