| **Devi Ahilya University, Indore, India Institute of Engineering & Technology** | | | | **IV Year B.E. (Electronics and Telecommunication Engg.)** | | | |
|---|---|---|---|---|---|---|---|
| **Subject Code & Name** | **Instructions Hours per Week** | | | **Credits** | | | |
| **7ETRE1 SoC DESIGN AND VERIFICATION** | **L** | **T** | **P** | **L** | **T** | **P** | **Total** |
| | **3** | **1** | **2** | **3** | **1** | **1** | **5** |
| **Duration of Theory Paper: 3 Hours** | | | | | | | |

## Course Learning Objective:

- To Make the Student Understand Advanced Digital System Design using Verilog Programming and physical design flow
- To Make the Student Understand of various verification step in VLSI physical design and how to resolve any error during verification.

**Prerequisites:** Basic knowledge of Digital Design and VERILOG,

### COURSE CONTENTS

**Unit – 1**

**Physical Design flow:**

Detailed steps in Physical Design flow: Guidelines for floor plan, Placement, CTS, and routing ECO flow, signal integrity issues, physical verification, signoff DRC and LVS, ERC, IR Drop analysis, Antenna check, Electro-Migration analysis and ESD analysis. Physical design essentials an ASIC design implementation.

**Unit – 2**

**Timing Analysis I:**

Timing Parameter Definition – Setup Timing Check- Hold Timing Check- Multicycle Paths- False Paths - Clocking of Synchronous Circuits. timing classification of digital systems.

**Unit – 3**

**Timing Analysis II:**

Synchronous Design - Origins of Clock Skew/Jitter and impact on Performance - Clock Distribution Techniques - Latch based clocking - Clocking tree topologies: H-tree, X-tree. Elmore delay model to calculate skew- Buffer insertion in clock trees- Exact Zero skew clock routing algorithm.

**Unit – 4**

Introduction of SOC Verification, Verification guidelines: Verification Process, Introduction of System Verilog, Basic Test bench functionality, Data types , Array (Packed & Unpacked Array, Dynamic, Associative & Queue Array), Procedural Statement and Control Flow

(Loop's, Blocking and Non-blocking Statements), Task and Function, Randomization & Constraints, Inter Process Communication (Semaphore, Mailbox), Program Block and Clocking Block.

**Unit – 5**
Introduction of OOPs Concept (Class & Object, Constructor, this & super keyword, Inheritance, Polymorphism), Copy Method (Shallow & Deep Copy), Coverage (Functional and Code Coverage), Assertions (Immediate & Concurrent Assertions).

## Course Outcome:

Students earned credits will develop ability to

| **CO. No.** | **CO** | **PO** |
|---|---|---|
| **CO1** | Understand the physical design flow and its essential steps, including floor planning, placement, CTS, routing, and physical verification. | PO1, PO2, PO3 |
| **CO2** | Analyze timing parameters and perform timing verification, including setup/hold checks, clock skew, and jitter analysis. | PO1, PO2, PO4 |
| **CO3** | Design advanced digital systems using Verilog HDL and optimize clock | PO3, PO5, PO9 |
| **CO4** | Apply verification techniques using System Verilog, including testbench creation, randomization, and functional coverage. | PO2, PO4, PO5 |
| **CO5** | Implement OOPs concepts in verification, including classes, inheritance, polymorphism, and assertions. | PO2, PO5, PO10 |

## CO-PO Relationship

| CO | PO-1 | PO-2 | PO-3 | PO-4 | PO-5 | PO-6 | PO-7 | PO-8 | PO-9 | PO-10 | PO-11 | PO-12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CO1 | 3 | 3 | 3 | | | | | | | | | |
| CO2 | 2 | 3 | | 3 | | | | | | | | |
| CO3 | | | 3 | | 2 | | | | 2 | | | |
| CO4 | | 3 | | 3 | 2 | | | | | | | |
| CO5 | | 2 | | | 3 | | | | | 2 | | |
| | | | | | | | | | | | | |

## BOOKS RECOMMENDED:

[1]. Rabaey, Jan M. Digital integrated circuits a design perspective.
[2]. 1. Kahng, A.B., Lienig, J., Markov, I.L., Hu, J., "VLSI Physical Design: From Graph Partitioning to Timing Closure", Springer.
[3]. 2. Sherwani, N.A., "Algorithm for VLSI Physical Design Automation", 2nd Ed., Kluwer.

[4]. 3. J. Bhasker and Rakesh Chadha, "Static Timing Analysis for Nanometer Designs A Practical Approach" Springer 2009
[5]. D. D. Gajski, N. D. Dutt, A.C.-H. Wu and S.Y.-L. Lin, High-Level Synthesis: Introduction to Chip and System Design, Springer, 1st edition, 1992.
[6]. S. Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, Prentice Hall, 2nd edition, 2003.
[7]. G. De Micheli. Synthesis and optimization of digital circuits, 1st edition, 1994.
[8]. M. Huth and M. Ryan, Logic in Computer Science modeling and reasoning about systems, Cambridge University Press, 2nd Edition, 2004 5. Bushnell and Agrawal, Essentials of Electronic Testing for Digital, Memory & Mixed-Signal Circuits, Kluwer Academic Publishers, 2000

## List of Practical Experiments: