DEVI AHILYA VISHWAVIDYALAYA, INDORE

FACULTY OF ENGINEERING

SCHEME OF EXAMINATION
&
COURSE OF CONTENTS

M. E. (Electronics)
(Specialization in Digital Instrumentation)
Part Time

INSTITUTE OF ENGINEERING & TECHNOLOGY
(www.iet.dauniv.ac.in)

DEVI AHILYA VISHWAVIDYALAYA, INDORE
INSTITUTE OF ENGINEERING & TECHNOLOGY
ME (Electronics Engineering)(Part Time) With Specialization in **Digital Instrumentation**
Schemes of Subjects & Examination (Subject to revision)

Th Marks (Max 100,Min 50) shall be based on Theory paper-It shall be an examination in the end of the semester.
CW Marks (Max 50, Min 25) shall be based on Attendance (25), Marks obtained in Test-I & Test-II of 25 marks each. Average of the two tests will be taken for awarding the 25 marks.
SW Marks (Max 50, Min 25) shall be based on Attendance (25), Marks obtained in Two Experiments and Viva Voce (25)
Pr Marks (Max 50, Min 25) shall be based on Viva-Voce by External Examiner.
Th- Theory, CW – Class Work, SW – Sessional Work, Pr – Practical

Semester I

						Maximum Marks				
SNo	**Sub Code**	**Subject**	**L**	**T**	**P**	**Th**	**CW**	**SW**	**Pr**	**TOTAL**
1.	5EI331	Advance Computer Networking	3	1	-	100	50	-	-	150
2.	5EI332	Embedded Microcontroller	3	1	2	100	50	50	50	250
3.	5EI333	Digital Control System	3	1	2	100	50	50	50	250
4.	5EI340	Comprehensive Viva-I	-	-	-	-	-	-	-	50
	TOTAL		**9**	**3**	**4**	**300**	**150**	**50**	**50**	**700**

Semester II

SNo	**Sub Code**	**Subject**	**L**	**T**	**P**	**Th**	**CW**	**SW**	**Pr**	**TOTAL**
1.	5EI334	Process Instrumentation Systems	3	1	2	100	50	50	50	250
2.		Elective-I	3	1	-	100	50	-	-	150
3.	5EI341	Comprehensive Viva-II	-		-	-	-	-	-	50
	TOTAL		**6**	**2**	**2**	**200**	**100**	**50**	**50**	**450**

Semester III

SNo	**Sub Code**	**Subject**	**L**	**T**	**P**	**Th**	**CW**	**SW**	**Pr**	**TOTAL**
1.	5EI381	Modeling, Simulation and Evaluation Techniques	3	1	-	100	50	-	-	150
2.	5EI382	Advance Digital Signal Processing	3	1	2	100	50	50	50	250
3.	5EI384	Programming Language for Instrumentation systems	3	1	2	100	50	50	50	250
4.	5EI390	Comprehensive Viva-III	-	-	-	-	-	-	-	50
	TOTAL		**9**	**3**	**4**	**300**	**150**	**50**	**50**	**700**

Semester IV

SNo	Sub Code	Subject	L	T	P	Th	CW	SW	Pr	TOTAL
1.	5EI383	VHDL for Instrumentation Systems	3	1	2	100	50	50	50	250
2.		Elective-II	3	1	-	100	50	-	-	150
3.	5EI391	Comprehensive Viva-IV	-	-	-	-	-	-	-	50
	TOTAL		**6**	**2**	**2**	**200**	**100**	**50**	**50**	**450**

Elective – I: Any one of the following (For II Semester)

						Maximum Marks				
SNo	**Sub Code**	**Subject**	**L**	**T**	**P**	**Th**	**CW**	**SW**	**Pr**	**TOTAL**
1.	5EI335	Advance Logic Design	3	1	-	100	50	-	-	150
2.	5EI336	Digital Instrumentation Technology	3	1	-	100	50	-	-	150
3.	5EI337	Software Engineering	3	1	-	100	50	-	-	150
4.	5EI338	Optical & Laser Instrumentation	3	1	-	100	50	-	-	150
5.	5EI339	Web Technology	3	1	-	100	50	-	-	150

Elective – II: Any one of the following (For IV Semester)

SNo	Sub Code	Subject	L	T	P	Th	CW	SW	Pr	TOTAL
1.	5EI385	Biomedical Instrumentation	3	1	-	100	50	-	-	150
2.	5EI386	Fuzzy Logic & Neural Network	3	1	-	100	50	-	-	150
3.	5EI387	Network Security	3	1	-	100	50	-	-	150
4.	5EI388	Computer Added Instrumentation	3	1	-	100	50	-	-	150
5.	5EI389	VLSI Technology	3	1	-	100	50	-	-	150

Semester V

					Maximum Marks				
SNo	**Sub Code**	**Subject**	**L**	**P**	**Th**	**CW**	**SW**	**Pr**	**TOTAL**
1.	6EI331	Dissertation Phase-I	-	8	-	-	100	50	150
	TOTAL		**-**	**8**	**-**	**-**	**100**	**50**	**150**

Semester VI

					Maximum Marks				
SNo	**Sub Code**	**Subject**	**L**	**P**	**Th**	**CW**	**SW**	**Pr**	**TOTAL**
1.	6EI381	Dissertation Phase-II	-	12	-	-	250	100	350
	TOTAL		**-**	**12**	**-**	**-**	**250**	**100**	**350**
		GRAND TOTAL OF SIX SEM.							**2800**

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Instrumentation) I – SEMESTER (Part Time)					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5EI331	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
Advance Computer Networking	**3**	**1**	**-**	**Max**	**100**	**50**	**-**	**-**	**150**
Duration of paper: 3 hrs				**Min**	**50**	**25**	**-**	**-**	**75**

Course Objectives:
Appreciate working network layer protocols, selection of appropriate routing algorithm, understanding of QOS parameters, understanding of transport and application layer protocols, use of cryptography in computer networking.

Prerequisite(s):
Fundamentals of computer networking, concepts of programming and operating systems.

COURSE OF CONTENTS

UNIT -I
Introduction and overview of OSI reference model TCP/IP reference model, Physical layer & its functions, Data link layer, MAC sub layer, their functions, overview of data link layer and Mac sub layer protocols (stop & wait, sliding window, aloha, CSMA, CSMA/CD, CSMA/CA).

UNIT -II
Network layer Design Issues, Routing Algorithms Shortest Path Routing, Flooding, Distance Vector Routing, Link State Routing, Broadcast Routing, Multicast Routing, and Routing in Ad Hoc Networks. Congestion Control Algorithms, General Principals , Prevention Policies, Congestion Control in, Virtual Circuit Subnets, Datagram Subnets, Load shedding, Jitter Control.

UNIT -III
Quality of Services, Requirements, Techniques for Achieving Q OS, Internetworking, Tunneling, and Internet work Routing, Network Layer in the Internet, IP Protocol, IP Addresses, OSPF, BGP, Internet Multicasting, Mobile IP IPV6.

UNIT -IV
Transport Service, Services Provided to Upper Layers. Transport Primitives, Berkeley Sockets, Elements of Transport Protocols, Addressing, Introduction to UDP, Introduction to TCP, TCP Service Model, TCP Protocol, TCP Segment Header. Performance Problems in Computer Networks, Network Performance Measurements. System Design for Better Performance.

UNIT -V
Various Application Layer Protocols DNS, SMTP, IMAP, WWW,
Introduction to Cryptography, Substitution Ciphers, Transposition Ciphers, Symmetric and Asymmetric Key Algorithms, DES, RSA, Digital Signature.

BOOKS RECOMMENDED
[1] A. S. Tanenbaum, *"Computer Networks",* 4th Edition Pearson Education, 2003.
[2] W. Stalling, *"Network Security and Cryptography",* 4th Edition Pearson Education, 2006.
[3] W. Stalling, *"Data & Computer Communication",* 8th Edition Pearson Education, 2006.

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Instrumentation) I – SEMESTER (Part Time)					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5EI332 **Embedded microcontroller**	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
	3	**1**	**2**	**Max**	**100**	**50**	**50**	**50**	**250**
Duration of paper: 3 hrs				**Min**	**50**	**25**	**25**	**25**	**125**

Course Objectives:

Designing microcontroller based hardware, understanding use of timers and interrupts in different applications ability to serially transmit-receive the data at standard baud rate with an interface, using microcontroller in industrial applications, embedded software architecture

Prerequisite(s):

Knowledge of microprocessor, peripherals, interfaces and assembly language programming

COURSE OF CONTENTS

UNIT -I

Microprocessor and microcontroller comparison, microcontroller survey, 8051 architecture General purpose registers, special function registers, input/output ports and circuits, internal memory connecting external memory, and I/O interface 8255 ,data transfer, arithmetic, logical, branch instructions, bit-related instructions , assembly language programming

UNIT -II

Interrupts, timer flag interrupt, serial port interrupt, external interrupt ,interrupt control, interrupt priority interrupt destination , software generated interrupts , counter and timers , timer modes of operation ,timing subroutines-pure software time delay, software polled timer, pure hardware delay, look-up tables

UNIT -III

Serial data communication, different modes , serial data transmission-reception using time delay , by polling , interrupt driven , microcontroller applications as interfacing with keyboard and display devices A/D and D/A converters , waveform generation , frequency and pulse width measurement, stepper motor control etc.

UNIT -IV

8051 family members as 8052 with capture timer , A/D and D/A equipped family members, watch dog timer , pulse width modulation, analog comparators, PIC 16C6X/7X,16 F8XX microcontroller and architecture , industrial applications of microcontroller

UNIT -V

Software architectures-Round robin, Round robin with interrupts, function-queue-scheduling, Real time operating system architecture – task states, scheduler, reentrancy, shared data problem, interrupt latency RTOS-semaphores and problems , inter –task communication with message queues, mailboxes and pipes, Basic design using real time operating system

BOOKS RECOMMENDED

[1] Mohamed. Ali Mazidi, Janice Ali Mazidi, Rolin D. McKinley, *"The 8051 microcontroller &r Embedded System*, 2nd Edition Pearson Education, 2006

[2] Kenneth J.Ayala, *8051 microcontrolle r*, Architecture*, Programming & Applications,* Penram international publishing (India) Pvt Ltd, 1996

[3] David E. Simon, *An Embedded software Primer*, Ist Pearson education, 1999

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Instrumentation) I – SEMESTER (Part Time)					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5EI333 **Digital Control System**	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
	3	**1**	**2**	**Max**	**100**	**50**	**50**	**50**	**250**
Duration of paper: 3 hrs				**Min**	**50**	**25**	**25**	**25**	**125**

Course objective:
To control a continuous-time (analogue) dynamical system using a digital operational element such as a digital computer. The aim is to give students a clear understanding on characteristics of digital control systems from both frequency and time domain viewpoints.

Prerequisite(s):
Knowledge of classical control methods & MATLAB control system toolbox

COURSE OF CONTENTS

Unit-I
Advantages& disadvantages of digital control, Elements, Block diagram, Difference equations, Sampling process and its frequency domain analysis, Ideal sampler, Sampling theorem & Nyquist frequency, Data conversion techniques, Data reconstruction, Type of Holds :Zero order & First order .

Unit-II
Definition and determination Z-transform, Mapping between S-plane and Z-plane, Z-transform theorems, The inverse Z-transform, Z-transform of system equations, Solution of linear difference equations using Z-transform, The pulse Transfer function, Block diagram reduction for systems interconnected through samplers, Sampled Signal flow graphs.

Unit-III
Stability studies using Routh's test & Jury's test, Steady state error Analysis for discrete time system, Root locus Analysis, Correlation between time Response & frequency response, Effect of adding pole & zero to open loop transfer function.

Unit-IV
State variable representation, Time domain state and output equations for sampled data control system, State Model of a discrete time SISO system using phase variables - canonical variables - physical variables, State transition equation, State variable representation in the z-domain, System stability, Relation between state equation & transfer function. Time response between sampling instants.

Unit-V
Digital design of digital controllers, Realization of digital PI, PD, PID controllers.

Books Recommended:

[1] Kuo B.C. "*Digital Control System*", 2nd Edition Oxford Press, 1992.
[2] Ogata K, "*Discrete – Time Control System*", 2nd Edition PHI, 1995.
[3] Franklin G.F. and Powell J.D., *Digital Control of Dynamic Systems*, Addison-Wesley, 1980.
[4] Gopal M. "*Digital Control System*", TMH, 1997.

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Instrumentation) II – SEMESTER (Part Time)					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5EI334 **Process Instrumentation System**	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
	3	**1**	**2**	**Max**	**100**	**50**	**50**	**50**	**250**
Duration of paper: 3 hrs				**Min**	**50**	**25**	**25**	**25**	**125**

Course Objectives

To develop fundamentals of process control characteristics and various process schemes. To formulate approaches for the process/modification, control structure design and algorithm tuning to achieve good performance over a range of operating conditions.

Prerequisite(s):

Basic principles of Sensors and Transducers

COURSE CONTENTS

Unit 1: Process Characteristics & Automatic Controllers

Process Variables, Process Degree of Freedom, Characteristics of Physical System, Control System parameters, Continuous & discontinuous controller modes, Composite control mode, Analog & Digital controllers, Design of various kinds of controllers, Process Loop timing.

Unit-II: Hydraulic & Pneumatic Control system.

Concepts of resistance, capacitance, and inductors in liquid and pressure systems, Hydraulic and Pneumatic Components, Various kinds of controller & their characteristics, Thermal systems, Flow, pressure and level Control

Unit III: Complex Control Systems.

Introduction, cascade, feed forward, Ratio Control, Anti Reset, Selector & Multivariable control scanners, Final Control elements, Adaptor & Non linear Control System, Self Adaptive Systems, Predictive Approach

Unit IV: Programmable Logic Controllers

Discrete state Process Control , Discrete State Variable, Event Sequence Description , Ladder Diagram, Programmable controller, Relay Sequences, Programming, Advanced Features.

Unit V: Instrumentation in processing industry.

Instrumentation as applied to petro-chemical industry and thermal power plants, Overall plant description, Control of batch reactor, distillation columns, Furnace control, steam temperature control

Books Recommended:

[1]. D.P. Eckman "*Automatic Process control"*
[2] Patranabies "*Principles of Process control"*
[3] F.G. Shinskey. "*Process control System"*
[4] Curtis Johnson "*Process control Instrumentation Technology"*
[5] B.G. Liptak."*Hand Book of Process control"*
[6] Otter, Prentice Hall, 1988 "*Programmable logic Controllers",*

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Instrumentation) II – SEMESTER (Part Time)					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5EI335 (Elective) **Advanced Logic Design**	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
	3	**1**	**-**	**Max**	**100**	**50**	**-**	**-**	**150**
Duration of paper: 3 hrs				**Min**	**50**	**25**	**-**	**-**	**75**

Course Objective:
To provide an in-depth knowledge regarding designing of advance digital circuits. To emphasize on FSM based sequential circuit design and analysis of designed circuits for timing and performance.

Prerequisite:
Knowledge of basic digital electronics and state diagrams.

COURSE OF CONTENTS

Unit-I
Background for Digital Design
Logic Function Representation and Minimization, K-Map Minimization,EV- K-Map Minimization, Function Minimization by Using K-map XOR Patterns and Reed-Muller Transformation

Unit-II
Combinational Logic Design
Nonarithmetic Combinational Logic Devices –Multiplexers, Decoders, Encoders, De-Multiplexers, Code Converters, Magnitude Converters, Parity Generators and Error Checking Systems, Combinational Shifters, Steering logic and Tri-state gate application.
Arithmetic Devices – Binary adders and substractors, Carry Look ahead Adder, Multiple -number addition and Carry save adder, Multipliers, Parallel Dividers, Dedicated ALU design featuring RC and CLA Capability, Mux approach to ALU Design, Dual Rail system and ALU with completion signals.
Propagation Delay and Timing Defects in Combinational Logic.

Unit-III
Introduction to Synchronous State Machine Design and Analysis
Models for Sequential Machines, Basic Memory Cell, Flip-flop, Flip-Flop Conversions, Asynchronous Preset and Clear overrides, Latches and Flip-flop Timing Problems, Design of Synchronous state machine, Detection and elimination of output race glitches, static hazard in output logic, Clock Skew, Switch debouncing circuit, ASM chart and state tables.
Module and Bit-Slice Devices- Registers, Synchronous binary counters, Shift register counters, Asynchronous counters.

Unit-IV
Asynchronous State Machine Design and Analysis
Features of Asynchronous FSM, Lumped path delay models, Excitation table for LPD model, State diagram, state table and excitation table for Asynchronous FSM, Basic cell design using LPD model, Design of RET Flip-flops, Detection and elimination of timing defects, single transition time machines, Hazard free design, One Hot Design for asynchronous FSM.

Unit-V
Advance Sequential Designs
Externally Asynchronous/ Internally Clocked systems and Applications, Asynchronous Programmable Sequencers, One –hot Programmable asynchronous sequencers, Pulse mode approach to asynchronous FSM Design.

Books Recommended:
[1] Richard.F.Tinder, "*Engineering Digital design"*, 2nd Edition, 2000, Academic Press.
[2] William I. Fletcher, " *An Engineering Approach to Digital Design* " , Prentice Hall of India, 1996.
[3] James E. Palmer, David E. Perlman, *" Introduction to Digital Systems* ", Tata McGraw Hill, 1996.
[4] N.N. Biswas, *" Logic Design Theory* ", Prentice Hall of India, 1993.

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Instrumentation) II – SEMESTER (Part Time)					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5EI336 (Elective)	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
Digital Instrumentation Technology	**3**	**1**	**-**	**Max**	**100**	**50**	**-**	**-**	**150**
Duration of paper: 3 hrs				**Min**	**50**	**25**	**-**	**-**	**75**

COURSE OF CONTENTS

UNIT –I

Transducer Fundamentals: Classification, construction, design & performance characteristics, criteria for selection, working principle of Capacitive, LVDT, Piezo-Electric transducer.

UNIT –II

Strain and &Temperature measurement: Strain Gauges and Strain Measurement, Signal conditioning of strain gauges, non-electrical and electrical method for temperature measurement, high temperature measurement.

UNIT –III

Pressure Measurement: Manometers types, Mechanical Types, Elastic Types transducers, Low Pressure measurement gauges, measurement of vacuum using McLeod gauge, thermal conductivity gauges , Ionization gauge, Pirani gauge

UNIT –IV

Flow & level measurement: Theory of fixed restriction variable head type flow meters – orifice plate, venturi tube, flow nozzle, pitot tube, Rotameter, Principle and constructional details of electromagnetic flow meter, turbine flow meter, ultrasonic flow meters, direct and indirect method for level measurement, Electrical types of level gauges using resistance, capacitance, ultrasonic sensors.

UNIT –V

Virtual Instrumentation & Instrument drives: Data Acquisition system, SCADA systems, Distributed Digital Control system, Instrument drivers- GPIB bus, Field bus.

BOOKS RECOMMENDED

[1] Ernest O. Doebelin, *Measurement systems Application and Design*, International Student Edition, 4th Edition, McGraw Hill Book Company, 1998.

[2] R.K.Jain, *Mechanical and Industrial Measurements*, Khanna Publishers, New Delhi, 1999.

[3] A.K.Sawhney, A course in *Electrical and Electronic Measurement and Instrumentation* – Dhanpat Raj and Sons, New Delhi, 1999.

[4] Liptak B.G. *Instrument Engineers Handbook (Measurement)*, Chilton Book Co., 1994.

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Instrumentation) II – SEMESTER (Part Time)					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5EI337 (Elective) Software Engineering	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
	3	**1**	**-**	**Max**	**100**	**50**	**-**	**-**	**150**
Duration of Theory Paper: 3 Hours				**Min**	**50**	**25**	**-**	**-**	**75**

Course Objective:
To familiarize with the process of software development life cycle using the concepts of software engineering.

Prerequisites:
Knowledge of a programming language, preferably object oriented and a midsize project work

COURSE OF CONTENTS

Unit I
Software Engineering Process- Basic concepts of Software Engineering; Software life cycle; Role of Software Engineer; Application Domains, System Engineering; Software Quality.

Unit II
Software Design – Concepts of Analysis and Design; Object Orientation; Object Oriented Design; Design Issues; Case Studies.

Unit III
Verification and Validation – Testing; Debugging Analysis; Software Testing Strategies; Software Metrics.

Unit IV
Software Engineering Process Models - Different Models; Process Organization; Management planning control, Organization and Risk Management.

Unit V
Software Engineering Tools – System Programs, Role of Programming languages; CASE Tools; Objected Oriented Software Engineering; Reengineering process ,Client Server Software Engineering.

BOOKS RECOMMENDED:

[1] C.Gezzi, M. Jazayeri and D. Mandriohi *Fundament of software Engineering*, PHI 1996.
[2] R.S. Pressman, *Software Engineering A Practitioner Approch*, 4th Edition, Mcgraw Hill International Edition 20070
[3] P.Jalote, *An Integrated Approach to Software Engineering,* Naresa Publishing, latest Edition.
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Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Instrumentation) II – SEMESTER (Part Time)					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5EI338 (Elective) Optical & Laser Instrumentation	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
	3	**1**	**-**	**Max**	**100**	**50**	**-**	**-**	**150**
Duration of Theory Paper: 3 Hours				**Min**	**50**	**25**	**-**	**-**	**75**

COURSE OF CONTENTS

UNIT I

Optical Interferometry: Basics of interferometry, Study of common interferometers**,** Scientific and Engineering applications of Michelson interferometer, parallel plate, Fabry – Perot interferometer, grating shearing interferometers

UNIT II

Opto electronic devices: Optical Sources: Photo diode, PIN diode, schottky, barrier diode, heterojunction diode, APD, phototransistor, CCD and CMOS detectors and their application in analog and digital devices.

UNIT III

Elements of Lasers & applications: Measurement of distance, velocity, rotation, etc with lasers. Principle of LIDAR. Monitoring of clouds and atmospheric pollution. Laser as a heat source- its application in material processing and surgery.

UNIT IV

NDT using Optical techniques: Basics of Holography, speckle, photo-elasticity and moiré based techniques, Application of above techniques in detection of stress, strain, vibration, displacement, flow etc.

UNIT V

Optical fiber Sensors: Fiber basics, Multimode passive and active fiber sensors, phase and amplitude modulated sensors, Fiber systems sensing temperature, displacement, level, Flow, voltage, current and pressure

Text/References Books:

1. Wilson & Hawkes (1992) – *"Opto electronics"*, Prentice – Hall of Indian Pvt. Ltd.
2. A.Ghatak and K.Thyagarajan (1996) – *"Optical Electronic"*, Cambridge University Press.
3. 5. P. Bhattacharya (1997) – "*Semiconductor optoelectronic*" devices by, Pearson Education Asia group.
4. Jasprit Singh (1996) – "*Optoelectronic"* – An introduction to Materials and Devices by McGraw – Hill Companies International.
5. Culshaw B. and Dakin J.(Eds.), "*Optical Fibre Sensors" Vol I, II and III*", Artech House, 1989.
6. Fukuda, "*Optical Semiconductor Devices*", Allied Publishers Limited, Chennai, 1999.
7. Kasap, "*Optoelectronics and Photonics": Principles and practices*", Allied Publishers Limited, Chennai, 2001.
8. R.P.Khare, *"Fibre Optics and Optoelectronics", Oxford Press,* July 2004.
9. Djafar.K.Mynbaev, Lowell.L.Scheiner, "*Fiber-Optic Communications Technology*", 2nd Indian Reprint, Pearson Education Pte. Ltd., 2001.
10. Kasap, "*Optoelectronics and Photonics": Principles and practices*", Allied Publishers Limited,

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Instrumentation) II – SEMESTER (Part Time)					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5EI 339 Web Technology (Elective)	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
	3	**1**	**-**	**Max**	**100**	**50**	**-**	**-**	**150**
Duration of paper: 3 hrs				**Min**	**50**	**25**	**-**	**-**	**75**

Objectives:
Be familiarizing with the state-of-art technologies used for web development.

Prerequisites:
Basic Programming skills.

UNIT-1
Overview of Web Development – Web structure, need for careful web development, web process model, website design plan, Bita site implementation and testing; **HTML Basics –** Origin, HTML specification, structure and functions of HTML, elements and attributes, links and addressing.

UNIT-2
HTML Presentation and layout- text, lists, tables. Frames, Multimedia, Interactivity – Forms, CGI-browser server interaction, CGI output and Input , getting connected and publishing web site, Formatting Website with cascading Style Sheets.

UNIT-3
XML Basics – Elements & Attributes, Character data, Character & entity references, CDATA sections, processing instructions, document structure, XML parsers, XML declaration, XML Namespace, XML Schemas

UNIT-4
Transforming XML and DOM – What is Transformation, Executing Transformations, and XSLT for presentation: XML to HTML, DOM, DOM Implementation, DOM components.

UNIT-5
Web Services: Distributed Computing Architecture: DCOM, IIOP, RMI, Web services, web services stack: SOAP, WSDL and UDDI, Srvice oriented architecture.

RECOMMENDED BOOKS :

[1] Thomas A. Powell The complete Reference HTML & XHTML, 4th Edition, Tata McGraw-Hill, 2003.
[2] David Hunter, Beginning XML , 3rd Edition, Wiley Dreamtech,
[3] Frank P. Coyle, XML Web Services and Data Revolution, Pearson Education, 2002

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Instrumentation) III – SEMESTER (Part Time)					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5EI381 **Modeling Simulation and Evaluation Techniques**	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
	3	**1**	**-**	**Max**	**100**	**50**	**-**	**-**	**150**
Duration of paper: 3 hrs				**Min**	**50**	**25**	**-**	**-**	**75**

Course Objectives:

- To give exposure of stochastic processes and to show their importance in engineering education and research
- To develop skills to identify a process, its inputs and outputs. Then to develop a model and quantify the results.
- To give an hands on experience in MATLAB to be used as a simulation tool for the stochastic processes
- To develop an orientation towards research in electronics and computer engineering.

Prerequisite(s):
Fundamental knowledge of Probability Theory.

COURSE OF CONTENTS

UNIT –I
Introduction to Probability Theory - Relative Frequency and Classical Definitions, Sample Space and Events, Conditional Probabilities, Independent Events, Bayes Formula, Bernoulli Trials.

UNIT –II
Random Variables - Definition, Discrete and Continuous Random Variables, Cumulative Distribution Function(CDF), Probability Density Function (PDF), Distributions for Discrete and Continuous Random Variables, Geometric Distribution, Poisson Distribution, Uniform Distribution, Exponential Distribution, Normal Distribution, Mean, Variance and Moments of Random Variables, Function of a Random Variable and it's Expectation, Jointly Distributed Random Variable, Moment Generating Function.

UNIT –III
Markov Chains- Classification of stochastic process**,** Introduction to Markov chains, Classification of States, Transition Probabilities, Limiting State Probabilities, Higher Transition Probabilities, and Chapman Kol Mogorov Equation, Concept of Transient States and Absorption Probabilities, Solution of Problems Based on Markov Chains.

UNIT –IV
Markov Processes and Queuing Theory-Introduction to Continuous time Markov Chains, Birth and Death Processes, The Transition Probability Function, Limiting Probabilities, Non Birth Death Processes, Exponential Distribution & Poisson Process. Solution of Problems Based on Continuous Time Markov Chains, Introduction to Queuing Theory and M/G/1 Queuing Systems.

UNIT –V
Simulation- Simulation of Queues, Statistical Inference and Few Examples on Simulation.

BOOKS RECOMMENDED

[1] K.S.Trivedi*, "Probability and Statistics with Reliability, Queuing and Computer Science Applications*", 2nd Edition , A Wiley-Interscience Publication.
[2] Averill M. Law, W. David Kelton, "*Simulation Modeling and Analysis*"**,** 3rd Edition**,** Tata McGraw-Hill Publication.
[3] S.M. Ross, "*Introduction to Probability Models***,** 9th Edition**,** Elsevier Publication", 2007.
[4] A Papoulis, S.V Pillai, "*Probability Random Variables and Stochastic Processes*", 4th Edition, TMH Publication, 2002

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Instrumentation) III – SEMESTER (Part Time)					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5EI382 **Advance Digital Signal Processing**	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
	3	**1**	**2**	**Max**	**100**	**50**	**50**	**50**	**250**
Duration of paper: 3 hrs				**Min**	**50**	**25**	**25**	**25**	**125**

Course Objective:
To provide clear conceptual knowledge of different DSP algorithms and to introduce speech, multimedia and other signal processing applications.

Prerequisite(s):
A basic course in Digital signal processing.

COURSE OF CONTENTS

UNIT -I Signals and Signal Processing: Characterization and Classification of signals; Sampling and Quantization; Typical signal Processing Operations; Examples Typical Signals and Systems; Typical Signal Processing applications; Why Digital Signal Processing; Building blocks of a Digital signal processor; Discrete Time Fourier Transform, Z – transform and properties.

UNIT -II
Discrete Fourier Transform: Introduction; Computation of DFT and IDFT; Periodic and symmetry properties of DFT; DTFT v/s DFT; Circular shift and Circular convolution Linear convolution using DFT; Block convolution, Overlap – add method and Overlap – save method.

UNIT -III
Fast Fourier Transform: Redix Two DIT and DIF FFT algorithm; Butterfly computation; Bit reversed mapping; In place computation; Composite – N algorithm; Prime factor algorithm.

UNIT -IV
Digital Filter Structures: Block Diagram Representation; Signal Flow Graph Representation; Equivalent structures; Basic FIR Digital Filter structures; Basic IIR filter structures; state space structure; All Pass Filter; Tunable HR Digital filters; Cascaded lattice realization of IIR and FIR Filters; Parallel all Pass Realization of IIR Transfer Function; Computational Complexity of Digital Filter structures; Tellegen theorem and its applications.(Transposition theorem and Network sensitivity formula.)

UNIT -V
Digital Filter Design: Brief Review of Analog Filter Design; Impulse Invariance method of IIR filter design; bilinear Transform Method of IIR Filter Design; Design of Digital HR notch Filters; Low Pass HR digital filter design based on Truncated Fourier Series; FIR Filter Design Based on Frequency Sampling Approach; computer aided design of digital filters. Introduction to speech and language processing.

BOOKS RECOMMENDED

[1] Sanjit K. Mitra; *Digital Signal Processing A Computer- Based Approach*; 9th Edition, Tata McGraw Hill .
[2] V.K.Khanna;*Digital Signal Processing; Telecommunications and Multimedia Technology* Wheeler Publishing 1999.
[3] Richard G. Lyons Understanding *Digital Signal Processing*; .; First Indian Reprint ,Addison Wesely Longman Inc 1999.
[4] B. Somanathan Nair "*Digital Signal Processing, Theory, analysis and Digital filter design"*; PHI New Delhi India 2005.
[5] A. V. Oppenheim and R. W. Schafer "*Digital Signal Processing"*

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Instrumentation) III – SEMESTER (Part Time)					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5EI384	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
Programming Language for Instrumentation Systems	**3**	**1**	**2**	**Max**	**100**	**50**	**50**	**50**	**250**
Duration of paper: 3 hrs				**Min**	**50**	**25**	**25**	**25**	**125**

Course Objectives:
To understand and learn a programming language that expressly designed for use in the distributed environment of the technology along with an object-oriented programming model.

Prerequisite(s):
Knowledge Object Oriented Programming concept using object oriented languages such as C++, Objective C, Smalltalk, Eiffel, Common LISP Object System (CLOS), Object Pascal, and ADA 95 etc.

COURSE OF CONTENTS

UNIT -I
Introduction to Object Oriented Programming and Java :
Object Oriented Concepts, Abstraction, Encapsulation, Information Hiding. Java features: Java syntax, data types, data type conversions, control statements, operators and their precedence. Introduction to Class: Instance members and member functions. Concept of object initialization, constructors, constructor overloading. Access modifiers: Class attributes and methods

UNIT -II
Inheritance and Polymorphism
Class relationships: Inheritance and its types, Merits and Demerits, Polymorphism: Dynamic method dispatch, Runtime polymorphism, Abstract classes, Interfaces and packages.

UNIT -III
Exception Handling, Multithreading and Introduction to Java APIs:
Exceptions: Need for exceptions, Checked V/s Unchecked exceptions, creating exceptions.
Multithreading: Introduction, Priorities and scheduling, Thread Synchronization and its life cycle. String Handling, Wrapper classes: Arrays and Vectors

UNIT -IV
Java I/O, Applets and Event Handling:
Basic concept of streams I/O stream & reader-writer classes. File handling. Applet and its Life Cycle,
Basic GUI elements, Event Delegation Model and event handling

UNIT -V
Introduction to elementary procedures, Real & Complex vector and Matrix & Determinants and operations like: Initialization, Duplication, Elimination, Interchanging, Rotation, Norms, Scaling, Multiplication & calculation of rank etc.
Evaluation of various polynomials like Chebyshev polynomial, Fourier polynomial etc.
Analysis of real matrix problems like: Overdetermined systems, underdetermined system, homogenous, pseudo inversion. Sparse Real matrices, Similarity Transformation, Eigen value problems.
Numerical differentiation, Differential equations,
Introduction to special functions like: Exponential, Gamma, Error, Infinite time series, Fast Fourier transforms etc

BOOKS RECOMMENDED
[1]Hang T. Lau, *A Numerical Library in Java for Scientist & Engineers*, Library of Congress Cataloging-in-Publication Data by Chapman & Hall/ CRC Press Company.
[2] Cay S.Horstmann, *Core JAVA Vol-1*, Pearson Education.
[3] Herbert Schildt, *The complete Reference,* Tata McGraw Hill
[4] Kathy Sierra, *Bert Bates, Head First Java,* 2nd Edition, Oreilly

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Instrumentation) IV – SEMESTER (Part Time)					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5EI383 **VHDL for Instrumentation Systems**	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
	3	**1**	**2**	**Max**	**100**	**50**	**50**	**50**	**250**
Duration of paper: 3 hrs				**Min**	**50**	**25**	**25**	**25**	**125**

Course Objectives:
To enable the students to translate a functional system description into appropriate digital blocks coded in VHDL .Perform synthesis, place, and route of a digital design into a target FPGA

Prerequisite(s):
Digital Design, Microprocessor architecture, C++ language.

COURSE OF CONTENTS

UNIT -I Introduction to VLSI
History of IC Design, IC Technology, Moore's Law, IC Design Constraints, Feature Size, VLSI Family, Programmable Logic Devices, Designing with Programmable Logic- Design Entry, Simulation, Synthesis, Implementation, Device Programming, EDA Tools, IP Cores, Gjeski's Y Chart.

UNIT -II
FPGA and CPLD
ROMs, Logic array (PLA), Programmable array logic, GAL, bipolar PLA, NMOS PLA, PAL 14L4, Xilinx logic cell array (LCA) – I/O Block – Programmable interconnect – Xilinx – 3000 series and 4000 series FPGAs. Altera CPLDs, altera FLEX 10K series PLDs.

UNIT -III
Introduction to VHDL
Digital system design process , Hardware simulation , Levels of abstraction , VHDL requirements , Elements of VHDL Top down design, VHDL operators ,Timing ,Concurrency ,Objects and classes , Signal assignments ,Concurrent and sequential assignments.

UNIT -IV
Modeling Techniques and Advance Topics
Entity Declaration, Architecture Body, Process statement, Loop control statements, Multiple Processes, Delay Models, Signal Drivers, Block statements, Component declaration and Instantiation, Concurrent Assignment statements, Generics and Configuration, Subprogram, Overloading, Packages and Libraries, Design Libraries, Generate statements, Attributes, Hardware Modeling Examples: Modeling of digital modulator and demodulators, digital filters, WAP protocols, network security modules, wireless signal reception modules etc.

UNIT -V
Design for Synthesis
Language directed view of synthesis, Inference from CSA statements, Inference from within Process, Inference using Signals v/s variables, Latch v/s Flip Flop Inference, Wait statements, Synthesis Hints.

BOOKS RECOMMENDED

[1] P.K. Chan & S. Mourad, "*Digital Design sing Field Programmable Gate Array*" 1st Edition, Prentice Hall, 1994.
[2] J. V. Old Field & R.C. Dorf, " *Field Programmable Gate Array*", John Wiley, 1995.
[3] M. Bolton, "*Digital System Design with Programmable Logic*", Addison Wesley, 1990.
[4] Sudhakar Yalamanchili, "*Introductory VHDL- From Simulation to Synthesis* ",Pearson Education, 3rd Indian Reprint.
[5] Douglas Perry, "*VHDL*", 3rd Edition, McGraw Hill 2001.
[6] J. Bhasker, "*VHDL*", 3rd Edition, Addison Wesley, 1999.

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Instrumentation) IV – SEMESTER (Part Time)					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5EI385 (Elective) Biomedical Instrumentation	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
	3	**1**	**-**	**Max**	**100**	**50**	**-**	**-**	**150**
Duration of Theory Paper: 3 Hours				**Min**	**50**	**25**	**-**	**-**	**75**

Course Object-
Application of engineering principles to solving problems encountered in medicine and biomedical research. Topics include transducer principles, electrophysiology, and cardiopulmonary measurement systems. The laboratory project involves the design of a microcontroller and PC-based electrocardiograph is required to expand on the lab project.

Prerequisites:
Basic Knowledge of Physiological parameters, their measurement etc. Various systems of living beings.

COURSE CONTENTS

Unit I
Introduction to Biomedical Instrumentation: Biometrics, development of Biomedical Instrumentation, problems encountered in Bio-medical measurements, sources of Bio-electric potential, active and resting potentials. Introduction to the physiology of cardiac, nervous, muscular and respiratory systems

Unit II
Basic Bio-Medical Transducer Principles: Different types of transducers and their selection in bio-medical instrumentation, Bio-potential electrodes and Bio-chemical. Basic theory of Electrode, its types and selection criteria.

Unit III
Cardiovascular measurement: The heart out cardio vascular system, Measurement of blood pressure, Blood flow, Cardiac output and cardiac rate. Electrocardiography, Bioelectric Potential Recorders: Introduction and analysis of ECG, EMG & EEG, construction and working principles. Measurement of electrical activities in muscles and brain: Electromyography, Electroencephalograph and their interpretation.

Unit IV
Biomedical Measurements: Measurement of blood pressure, direct-indirect methods, heart rate, respiration rate and pulse rate measurements, body temperature measurements, ultrasonic blood flow meters, electromagnetic blood flow measurements.

Unit V
Patient Monitoring System: Besides and Central patient monitoring systems, elements of I.C. monitoring, Instrumentation for patient monitoring. Biological Simulators: Muscle simulators, pace makers and defibrillators, diathermy. X-ray and Radio isotopic Instrumentation, Diagnostic X-ray, CAT, medical use of isotopes.

BOOKS RECOMMENDED:

[1] John G. Webster, John Wiley, *"Medical instrumentation application and design"*, 1998
[2] Cromwell, *"Biomedical Instrument"*, Prentice Hall of India, New Delhi
[3] R.S. Khandpur, *"Handbook of biomedical instrument"*, TMH, 1997.
[4] Goddes & Baker, *"Principles of Applied Biomedical Instrumentation",* John Wiley, 1998.
[5] Carr & Brown-Pearson*, "Biomedical Instrumentation & Measurement"*, 1997

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Instrumentation) IV – SEMESTER (Part Time)					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5EI386 (Elective) **Fuzzy Logic and Neural Network**	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
	3	**1**	**-**	**Max**	**100**	**50**	**-**	**-**	**150**
Duration of paper: 3 hrs				**Min**	**50**	**25**	**-**	**-**	**75**

Course Objectives:
To provides an understandable approach to knowledge-based systems for problem solving by combining different methods of AI, fuzzy systems, and neural networks.

Prerequisite(s):
Overview of Artificial Intelligence and Digital systems.

COURSE OF CONTENTS

UNIT -I Fuzzy Set Theory and Fuzzy System:
Fuzzy sets, operations on fuzzy sets, intersections and unions, fuzzy relations, fuzzy compositions.
Extension principle, fuzzy numbers, arithmetic operations, approximate reasoning, fuzzy inference, linguistic model of complex systems, firing of rules.

UNIT -II
Introduction to Fuzzy Control :
Fuzzy control basics, relationship to PID control, construction of knowledge base, Mamdani and Sugeno fuzzy knowledge base controls, defuzzification, fuzzy control examples, fuzzy nonlinear simulation, genetic algorithms, tuning of fuzzy systems.

UNIT -III
Introduction to Neural Networks:
What is a Neural Network. Models of a Neuron. Network Architectures. Learning Processes.

UNIT -IV
Perceptron Model and Self Organising Maps:
Unconstrained Optimization Techniques. Linear Least-Squares Filters. Least-Mean-Square Algorithm. Perceptron. Back-Propagation Algorithm. XOR Problem. Generalization. Approximations of Functions.
Self-Organizing Map algorithm. Learning Vector Quantization.

UNIT -V
Fuzzy Neural Networks
Integration of fuzzy logic and neural networks ,Fuzzy Hybrid neural, Computation of fuzzy logic inferences by hybrid neural net,Trainable neural nets for fuzzy IF-THEN rules,Implementation of fuzzy rules by regular FNN of *Type 2* ,Implementation of fuzzy rules by regular FNN of *Type 3* ,Tuning fuzzy control parameters by neural nets,Fuzzy rule extraction from numerical data,Neuro-fuzzy classifiers,ANFIS,Applications of fuzzy neural systems.

BOOKS RECOMMENDED

[1] S. Haykin, "*Neural Networks: A Comprehensive Foundation*", Prentice Hall, 1999. Reference and Reading Materials:
[2] G J Klir and T A Folger, "*Fuzzy sets, uncertainty, and information*", Prentice-Hall, 1992.
[3] D. Driankov, H. Hellendoorn and M Reinfrank, "*An introduction to fuzzy control*", Springer-Verlag, 1993.
[4] G J Klir and B Yuan, "*Fuzzy Sets and Fuzzy Logic - Theory and Applications*", Prentice-Hall, 1995.
[5] C. Bishop, "*Neural Networks for Pattern Recognition*", Oxford University Press, 1995.

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Instrumentation) IV – SEMESTER (Part Time)					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5EI 387 (Elective) Network Security	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
	3	**1**	**-**	**Max**	**100**	**50**	**-**	**-**	**150**
Duration of Theory paper: 3 hrs				**Min**	**50**	**25**	**-**	**-**	**75**

Objectives:
Survey of principles and practice of network and system security to bring awareness about how to protect
data and resources from disclosure, guarantee the authenticity of data and messages and to protect the system from network-based attacks

Prerequisites:
Computer network, number theory, probability theory

COURSE OF CONTENTS

UNIT-1
Attacks, services and mechanisms, security attacks, security services model for network security Conventional Encryption model, Steganography, Classical Encryption Technique, modern Encryption Technique, Data Encryption Standard, Block Cipher design principles, Block Cipher mode of operation, Placement of Encryption Function, random number generation

UNIT-2
Authentication requirement, Authentication function , message authentication codes ,Hash function Security of Hash function and MAC's, Digital Signatures, Authentication Protocols , Digital Signature Standard

UNIT-3
Data security Architecture, confidentiality, integrity, availability, applications of data security architecture Wireless network security, radio frequency security basics, 802.11 security standard

UNIT-4
IP security overview, IP security architecture , Authentication Header, Encapsulating security Payload Web security requirement, secure sockets layer and transport layer security , secure electronic transaction

UNIT-5
System security ,Intruders , viruses and related threats ,Firewall design principles , Trusted system Network role- based security issues for E-mail, proxy server, web server, credit card security, printer and faxes

BOOKS RECOMMENDED

[1]William Stalling , "*Cryptography and Network Security"* Pearson education
[2] Roberta Bragg , "*Network Security-The complete reference" ,* Tata McGraw-Hill
[3]Charlie Kaufman, "*Network Security"* Eastern Economy Edition

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Instrumentation) IV – SEMESTER (Part Time)					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5EI388 (Elective) Computer aided Instrumentation	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
	3	**1**	**-**	**Max**	**100**	**50**	**-**	**-**	**150**
Duration of Theory Paper: 3 Hours				**Min**	**50**	**25**	**-**	**-**	**75**

Objectives:

1. Introduce students to the use of Labview, a commonly used tool for instrument control.
2. Develop a fundamental understanding of important issues encountered in instrumentation and device characterization, including accuracy, resolution, noise, parasitic, and grounding that will enable students to critically assess their data and to rapidly develop solutions to new measurement problems.
3. Encourage a systematic approach to the development of instrument control software, including overall planning, partitioning into testable and reusable pieces, incorporation of error detection and error handling, and provision of a user-friendly interface.

Prerequisite:

Overview of any programming language and database.

COURSE OF CONTENTS

Unit –I

Introduction to Labview: Computer-aided measurement systems; labview and data flow programming; virtual instruments-front panel and sub-vis as "subroutines"; controls and indicators; data types and conversions; operations on numbers; sequence, case, and while loops; running, stopping, and debugging vis; charts and graphs, arrays and cluster; strings and string manipulation; output to files and input from files; sub-vi creation; charts and graphs revisited and property nodes; state machines; some analysis vis; error-handling.

Unit -II

Basic measurements and Instrumentation Issues: voltage and current measurements; digitization, sampling, resolution, and accuracy; grounding; frequency and time measurements; waveforms and triggering; impedance measurements; noise and averaging; examples of sensors and devices, equivalent circuits for measurement systems; noise and interference; fundamental limitations on measurements; grounding.

Unit-III

DAQ interfacing and data acquisition: DAQ installation and interfacing; automation explorer;
analog input; analog output; digital input; digital output; buffering; applied averaging and analysis; essential vis.

Unit-IV

Instrument interfacing: GPIB characteristics; Visa vs. 488; automation explorer; controller, bus ID, listener, and polling; basic interchange and SRQ; instrument drivers and structure of packaged drivers; essential vis; other bus types (serial, USB); advanced concepts.

Unit-V

The user interface: who is the user? Guidelines for the user interface; advantages and disadvantages of particular user interface styles; other topics.

Books Recommended:

[1]. R.H. Bishop *"Labview(TM) 7.0 Express Student Edition with 7.1 Update"*, Prentice Hall, 2nd Edition, 2000
[2]. Rigby WH and T Dalby, "*Computer Interfacing: A Practical Guide to Data Acquisition and Control*", 1st Edition, Prentice Hall Inc. 1995
[3]. Doeblin, "*Measurement systems: Application and Design*", 4th Edition, McGraw Hill Inc., NY1990.

Devi Ahilya University, Indore, India Institute of Engineering & Technology				ME I Year Electronics(Sp. Digital Instrumentation) IV – SEMESTER (Part Time)					
Subject Code & Name	**Instructions Hours per Week**			**Marks**					
5EI389 (Elective) VLSI Technology	**L**	**T**	**P**		**TH**	**CW**	**SW**	**PR**	**Total**
	3	**1**	**-**	**Max**	**100**	**50**	**-**	**-**	**150**
Duration of paper: 3 hrs				**Min**	**50**	**25**	**-**	**-**	**75**

Course Objectives:
This course presents the fundamental of CMOS VLSI design with different VLSI design methodologies and combinational, sequential and semiconductor memory circuit design. It also covers the limitations of CMOS in NANO technology with introduction to the NANO Technology

Prerequisite(s):
Knowledge of semiconductor devices is required.

COURSE OF CONTENTS

UNIT -I
Introduction: VLSI design flow, VLSI design style, Fabrication process Flow: basic Steps, the CMOS n-well Process.
Metal oxide semiconductor (MOS) structure, Types of MOSFET: Enhancement and Depletion. Structure and operation of MOS transistor. MOSFET process simulation.

UNIT -II
MOS transistor: threshold voltage of MOSFET, controlling of threshold voltage, MOSFET current – Voltage Characteristics. Transconductance, Drain conduction. Aspect ration, process parameters, second order effects, MOS small signal and Large signal model, MOS capacitances.

UNIT -III
CMOS Inverter: Analysis of different types of inverter circuit, CMOS inverter, transfer characteristic, calculation of propagation delay, rise time, fall time, noise margin and power dissipation for CMOS Inverter. Effect of threshold voltage and supply voltage on Delay and power dissipation.

UNIT -IV
CMOS circuit Design: CMOS logic**,** pseudo NMOS logic, pass transistor logic, Transmission Gate logic and Dynamic logic circuit design. Designing of Combinational logic circuit, sequential logic circuit design and semiconductor memory circuit.

UNIT -V
Layout: Stick diagram rules for nMOS and CMOS technology, lambda based and micron based design rules. Layout design for CMOS inverter Circuit, circuit Extraction from Layout. Limitations of CMOS in NANO scale circuit design.

BOOKS RECOMMENDED

[1] Sung-mo Kang and Yusuf Leblebici, *CMOS Digital Integrated Circuit analysis and Design,* 3rd Edition, Tata McGraw-Hill.
[2] R. Jacob Baker, Harry W. Li and David E. Boyce, *CMOS Circuit design, layout and Simulation*, Series Edition, PHI, IEEE press,
[3] Yuan Taur and Tak H. Ning, *Fundamentals of Modern VLSI Devices*, Special Edition, Cambridge university press,1998
[4] Neil H.E. Weste and Kamran Esharhian, *Principal of CMOS VLSI design*,2nd Edition, PHI,.